

Compal Confidential

HM51_TR/HM70_TR Discrete

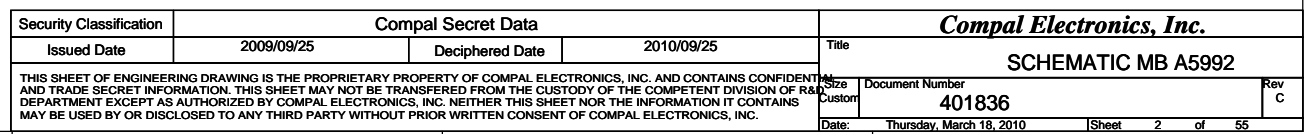
NDWG2/NDWH1 LA5992 Schematic Document

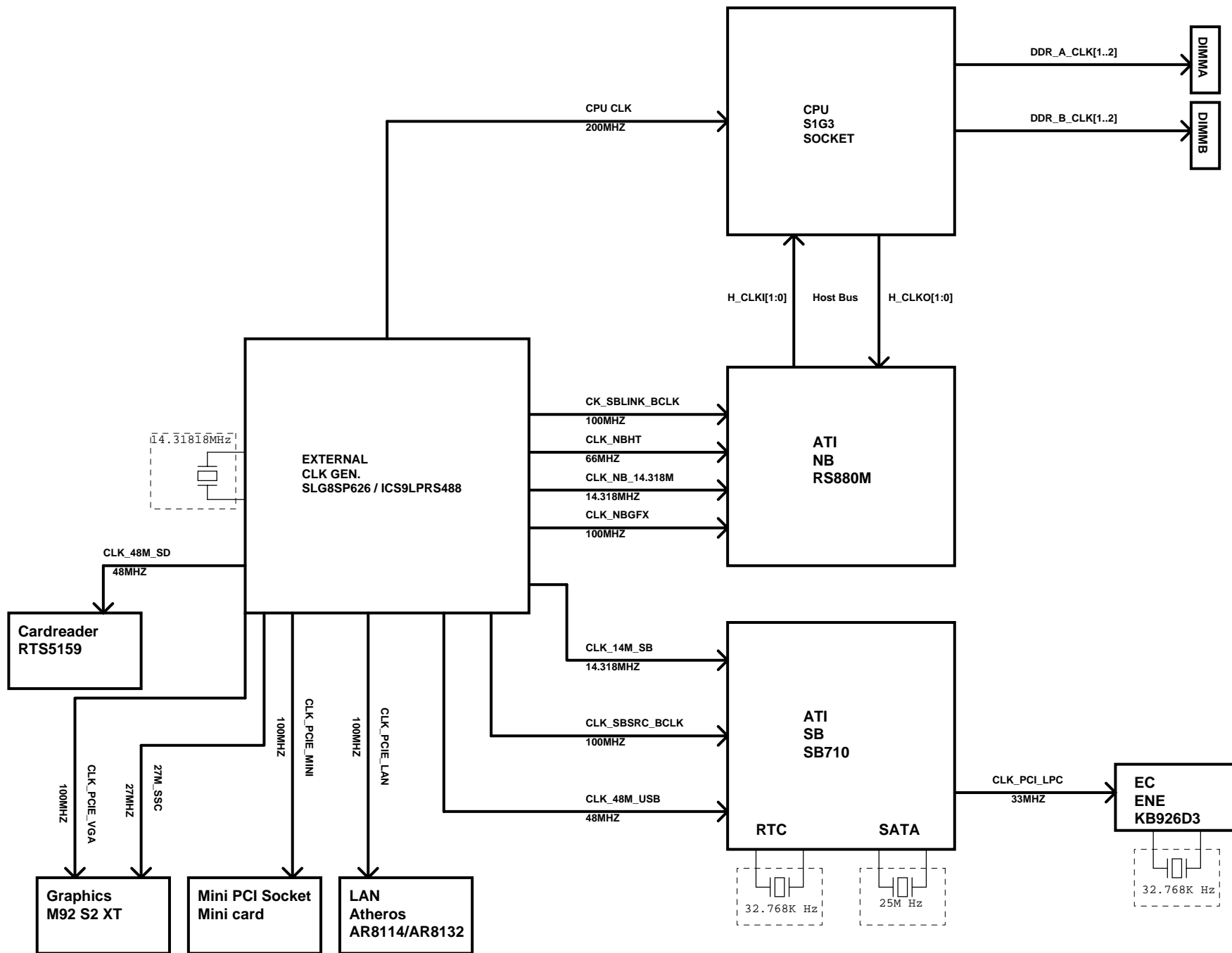
Mobile AMD S1G3/RS880M/SB710

2009/12/02 Rev 1.0

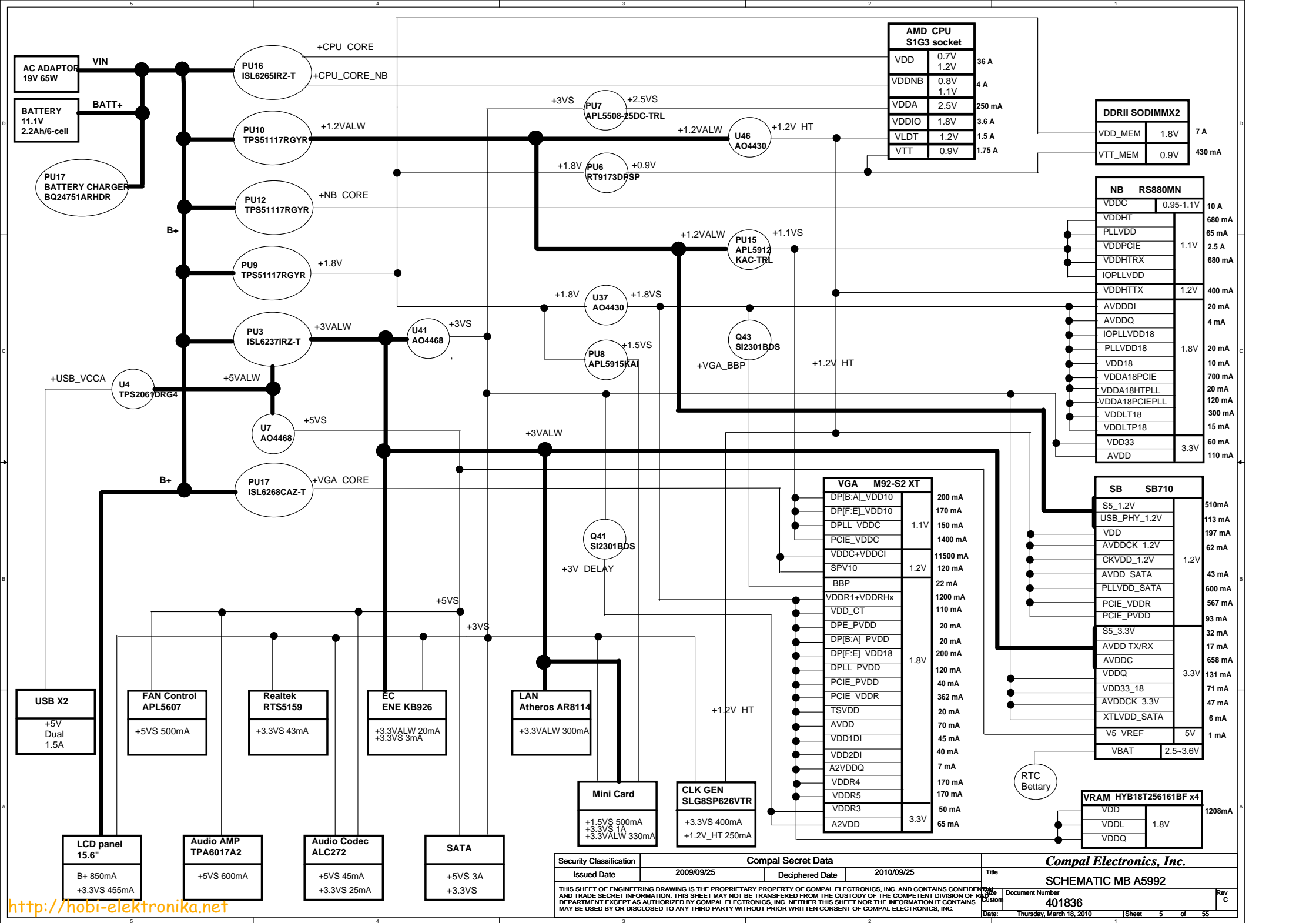
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Issued Date	2009/09/25	Deciphered Date	2010/09/25	Title	SCHEMATIC MB A5992
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File Name : LA-5992P





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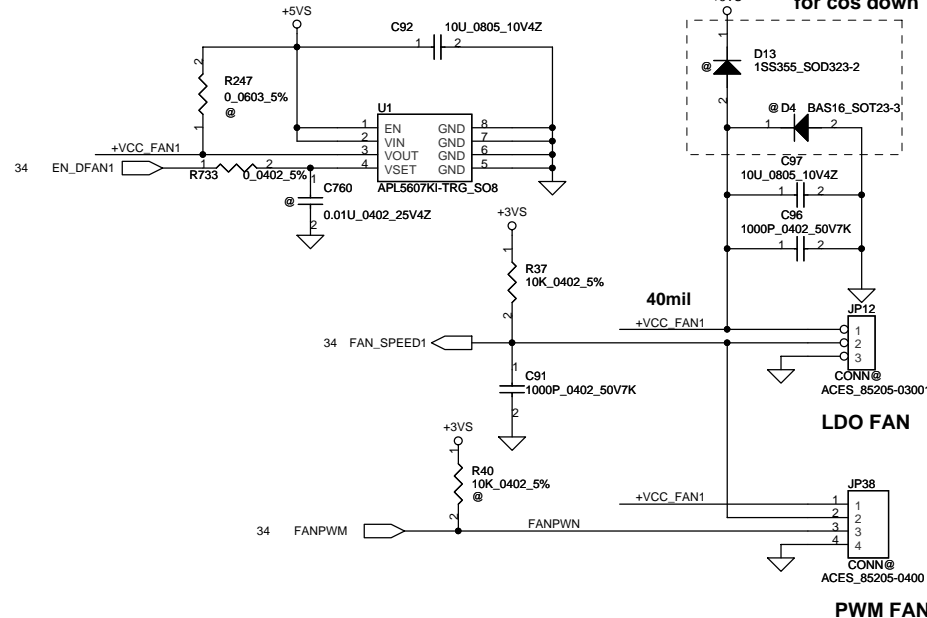
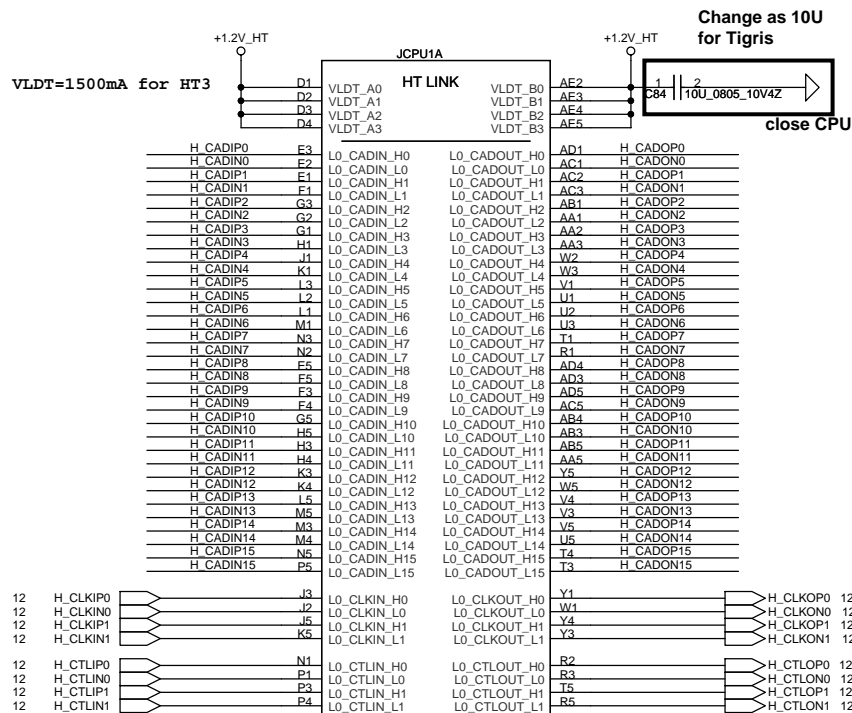


12 H_CADIP[0..15] H_CADIP[0..15]
12 H_CADIN[0..15] H_CADIN[0..15]

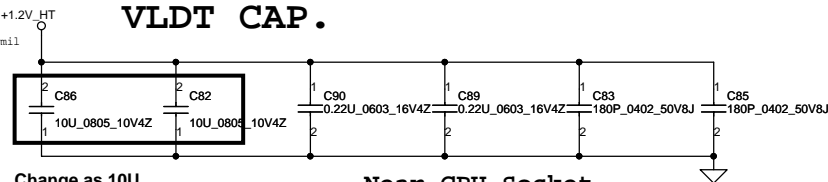
H_CADOP[0..15] H_CADOP[0..15] 12
H_CADON[0..15] H_CADON[0..15] 12

FAN Control Circuit

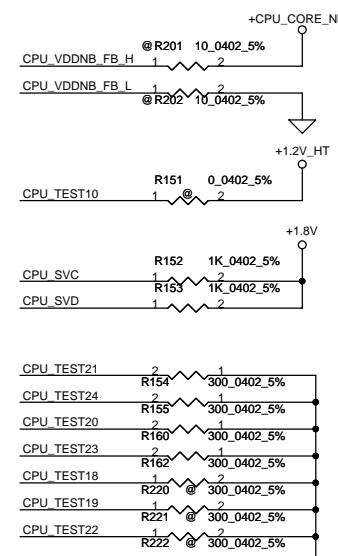
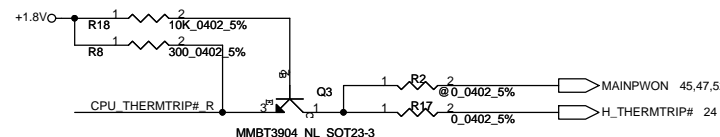
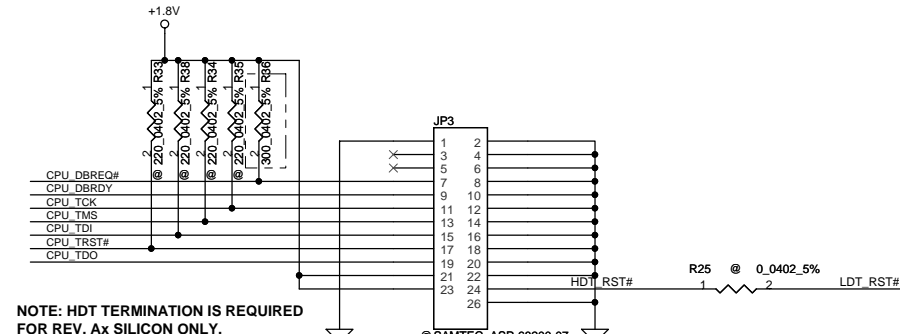
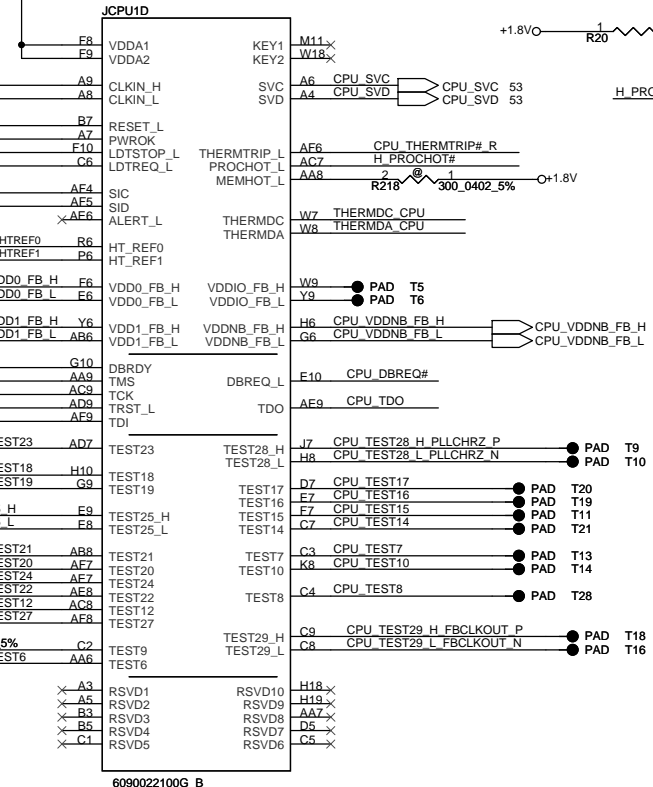
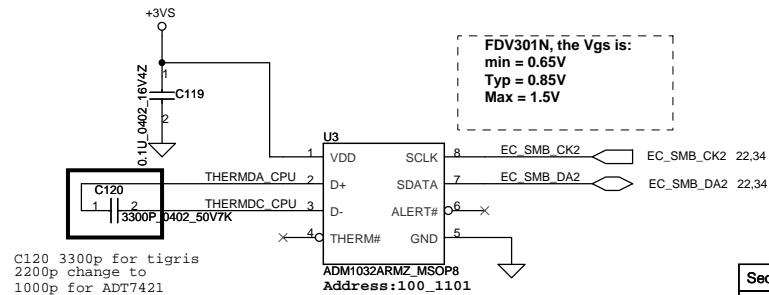
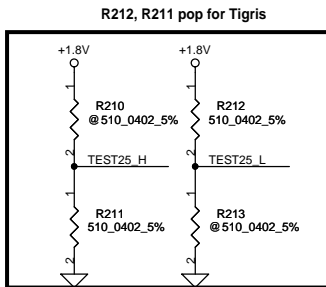
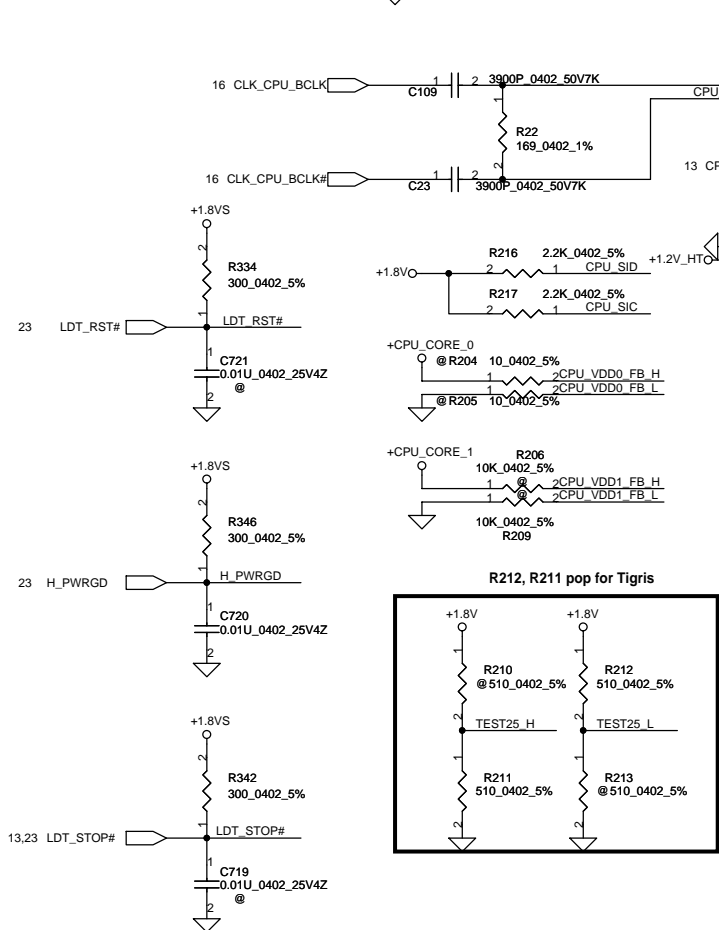
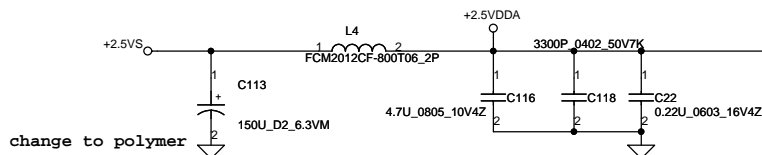
Reserve when PVT
for cos down



VLDT CAP.

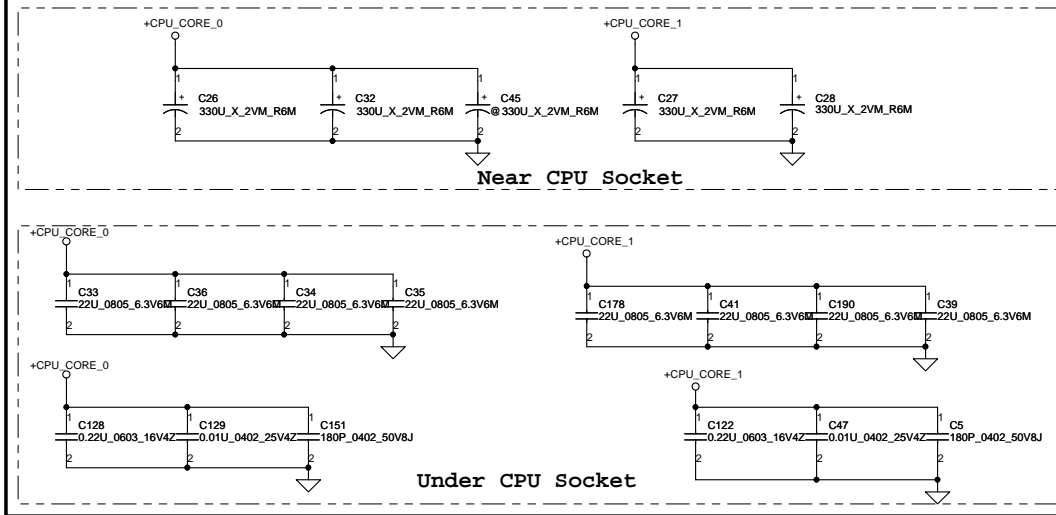


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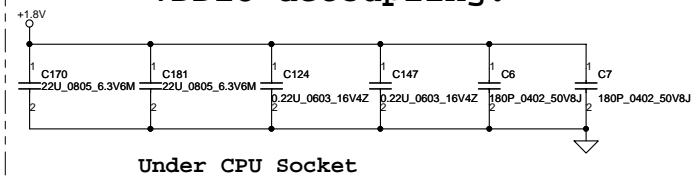


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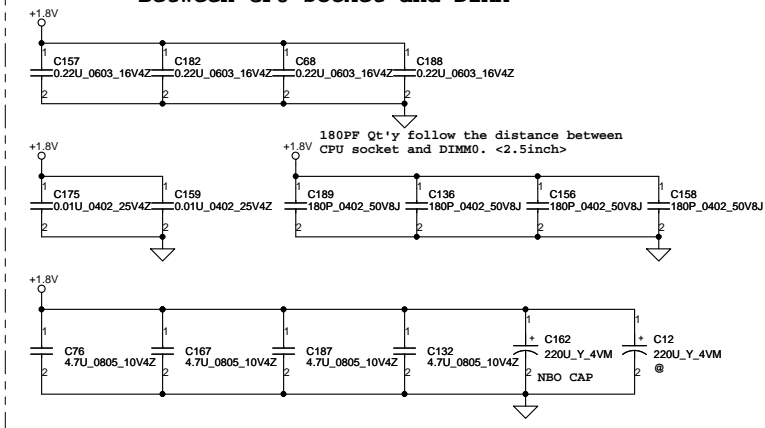
VDD(+CPU_CORE) decoupling.



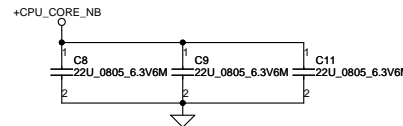
VDDIO decoupling.



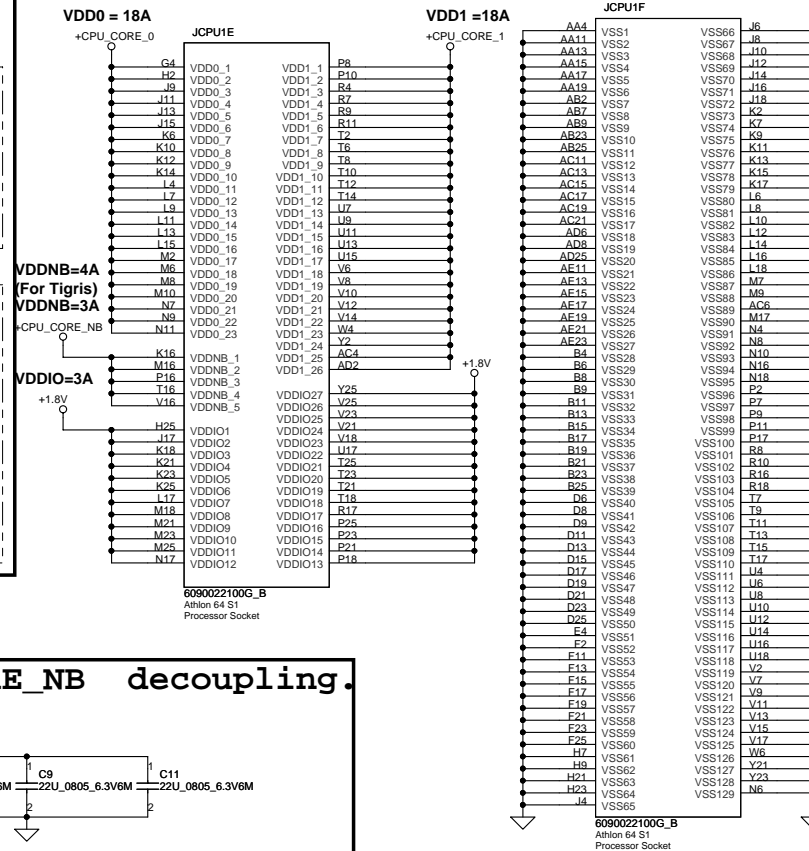
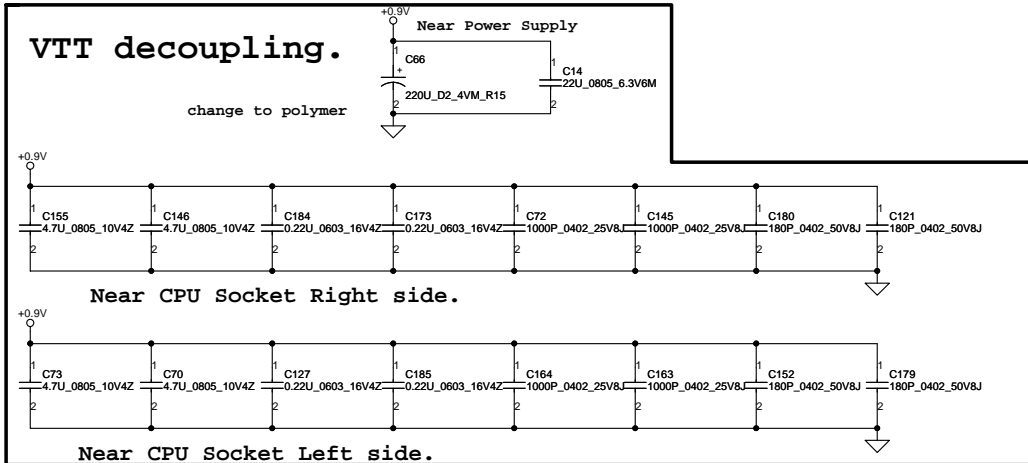
Between CPU Socket and DIMM



+CPU_CORE_NB decoupling.



VTT decoupling.



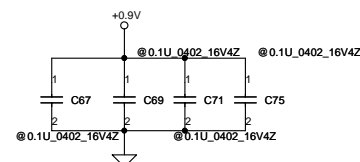
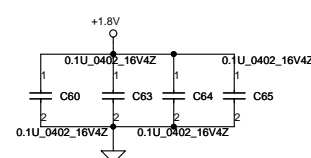
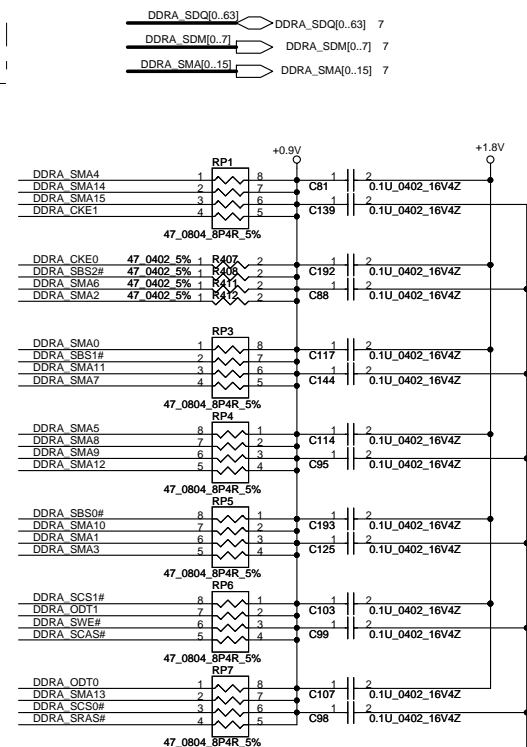
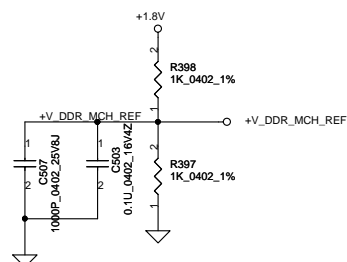
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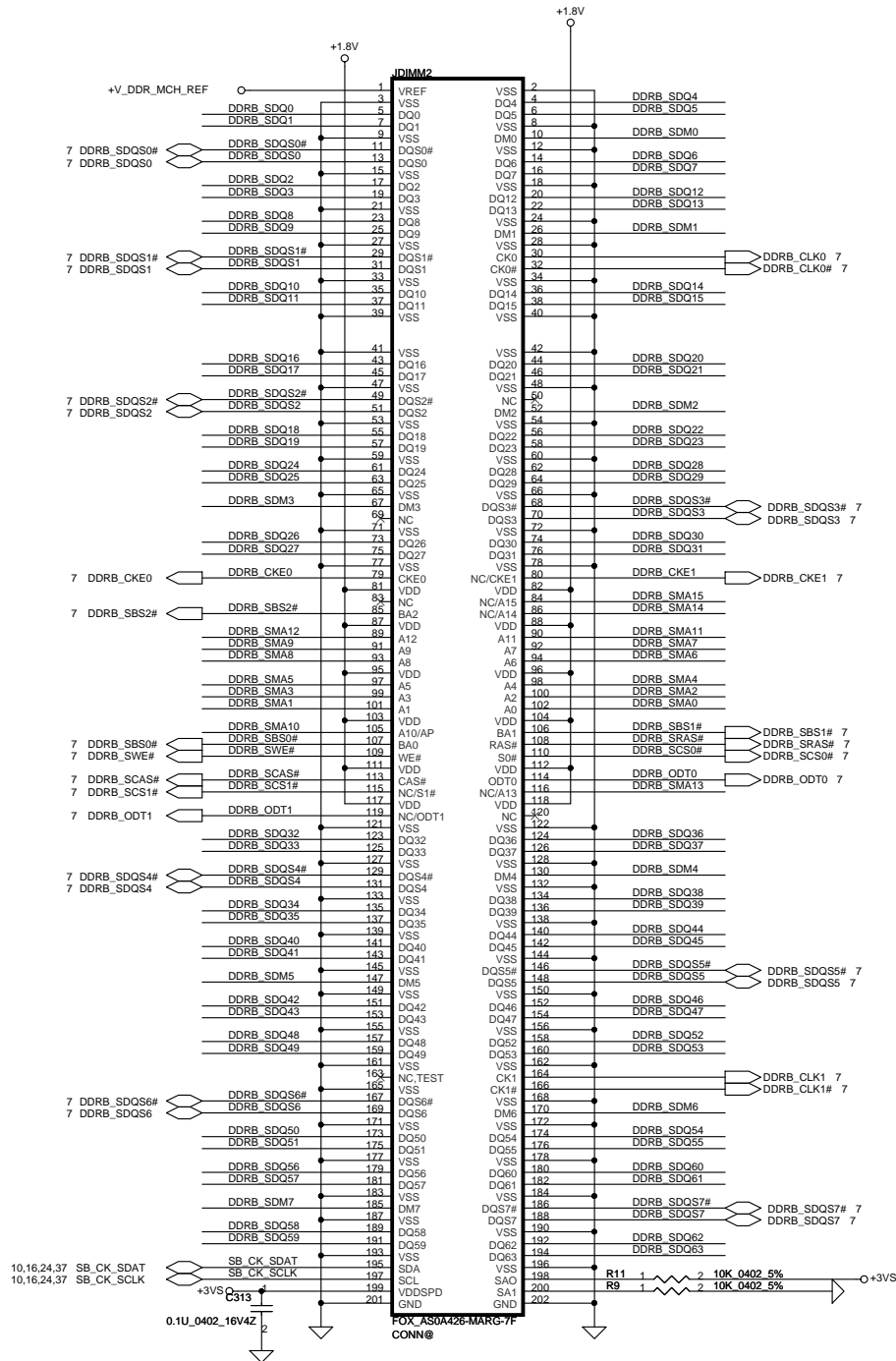
SCHEMATIC MB A5992

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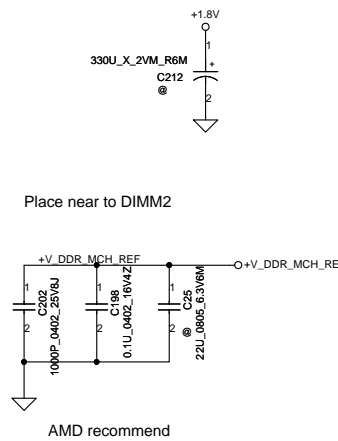
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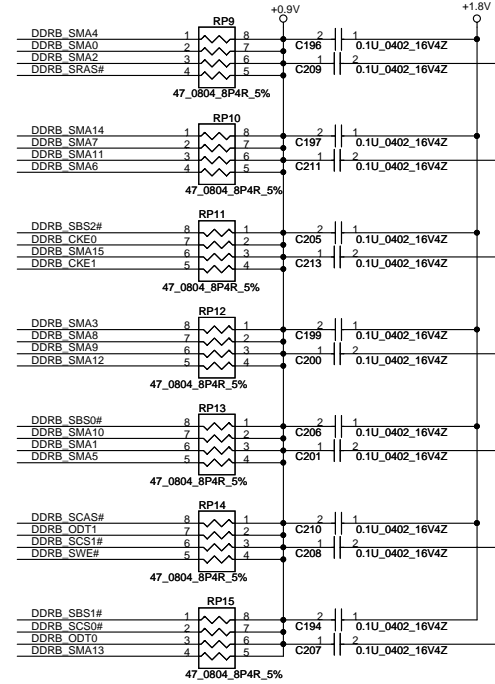
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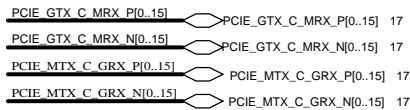
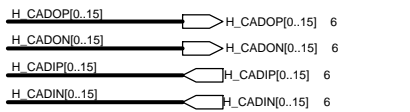
DIMM1 REV H:9.2mm (BOT)



DDR_B_SDQ[0.63] 7
DDR_B_SDM[0.7] 7
DDR_B_SMA[0.15] 7



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WLAN 37 PCIE_PTX_C_IRX_P0
LAN 31 PCIE_PTX_C_IRX_P1
31 PCIE_PTX_C_IRX_N1



PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

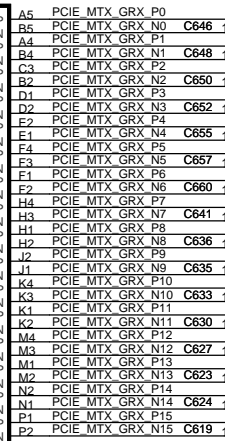
PCIE CALRP(PCE_BCALRP)
PCIE CALRN(PCE_BCALRN)

RS880M_FCBGA528

GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N
GPP_RX4P
GPP_RX4N
GPP_RX5P
GPP_RX5N

SB_RX0P
SB_RX0N
SB_RX1P
SB_RX1N
SB_RX2P
SB_RX2N
SB_RX3P
SB_RX3N

PCIE I/F SB



GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N
GPP_TX4P
GPP_TX4N
GPP_TX5P
GPP_TX5N

SB_TX0P
SB_TX0N
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SB_TX1N
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SB_TX2N
SB_TX3P
SB_TX3N

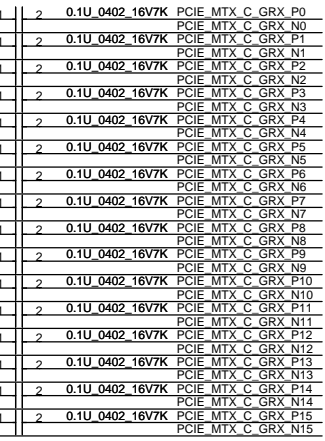
PCIE I/F SB



PCIE_ITX_C_PRX_P0
PCIE_ITX_C_PRX_P1
PCIE_ITX_C_PRX_N1

PCIE_ITX_C_PRX_P0
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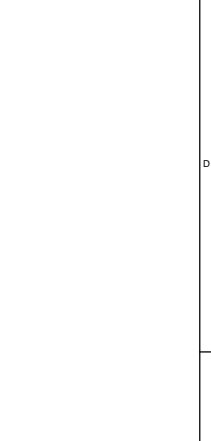
PCIE I/F SB



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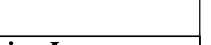
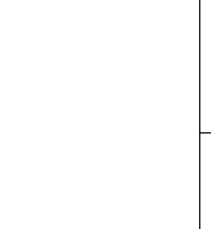
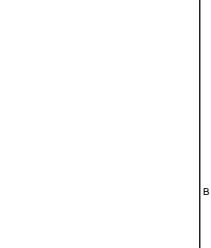
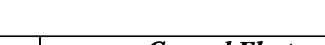
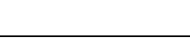
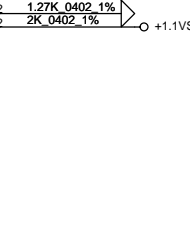
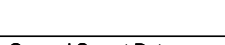
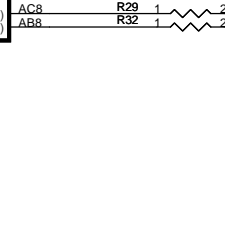
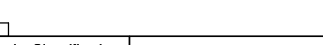
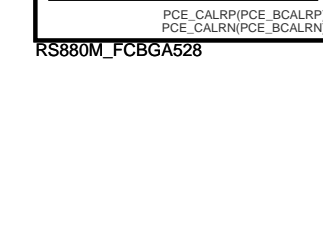
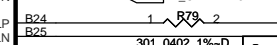
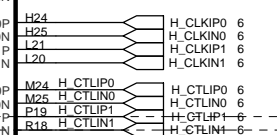
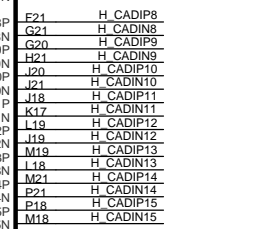
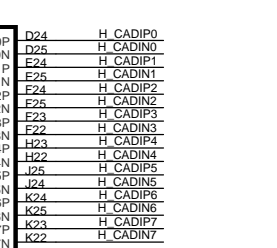
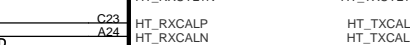
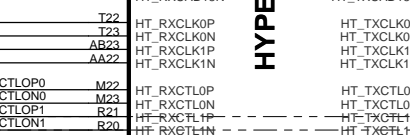
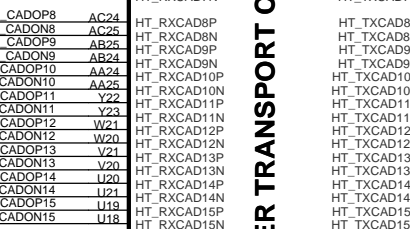
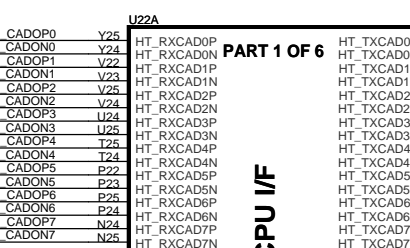
PCIE I/F SB



PCIE_ITX_C_PRX_P0
PCIE_ITX_C_PRX_P1
PCIE_ITX_C_PRX_N1

PCIE_ITX_C_PRX_P0
PCIE_ITX_C_PRX_P1
PCIE_ITX_C_PRX_N1

PCIE I/F SB



Place within 1" layout 4/8

HT Link
When time trace length, must keep 1:4 on self-trace

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Place within 1" layout 4/8

HT Link
When time trace length, must keep 1:4 on self-trace

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Place within 1" layout 4/8

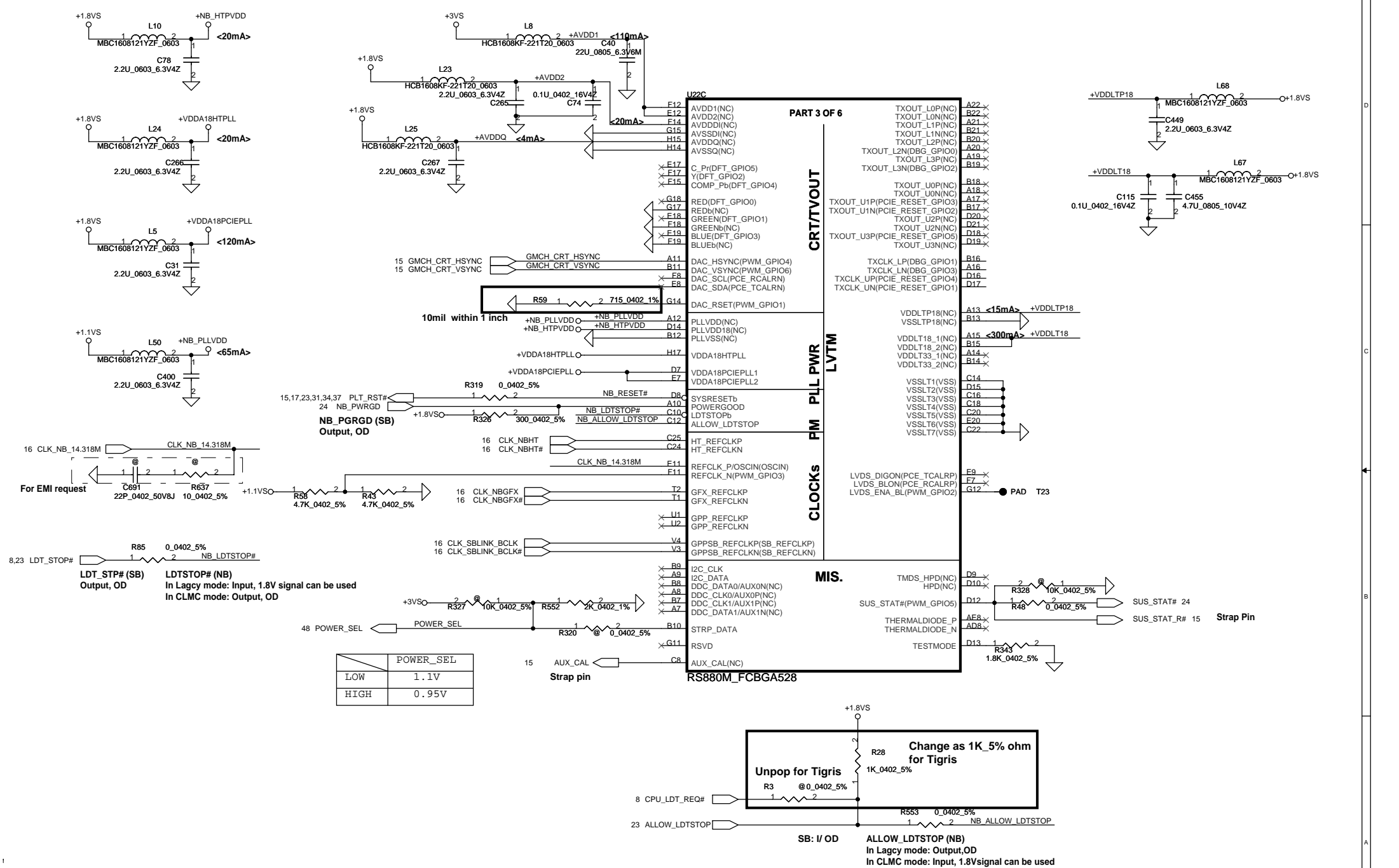
HT Link
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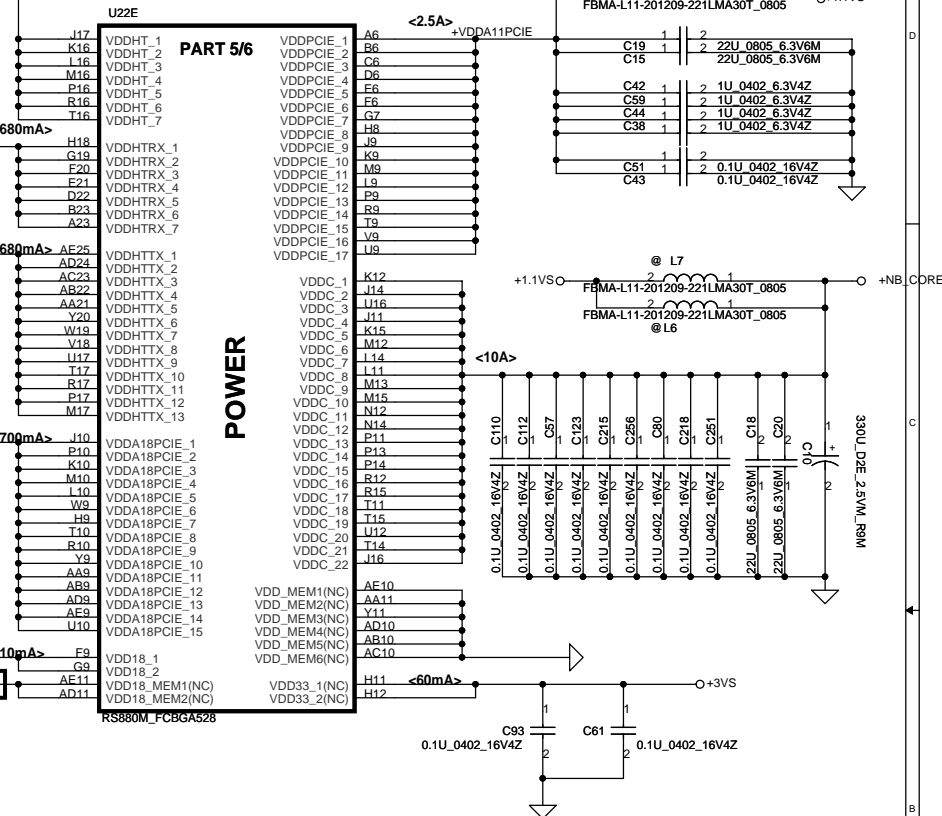
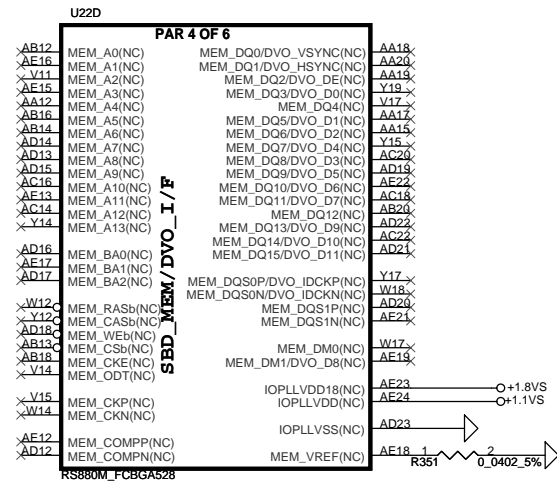
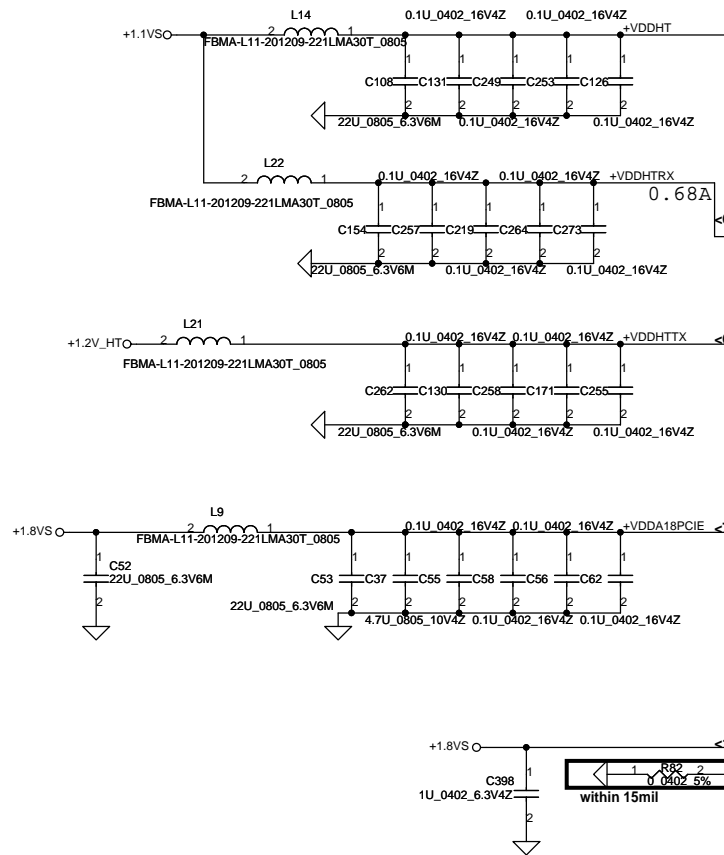
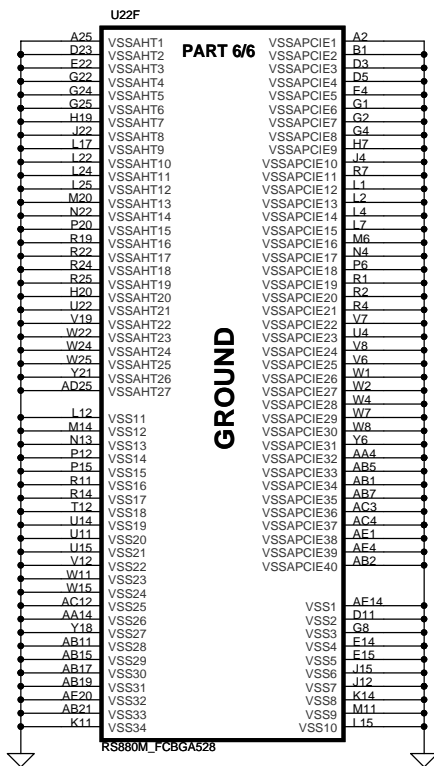
http://hobi-elektronika.net

Place within 1" layout 4/8

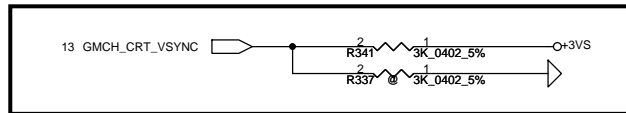
HT Link
When time trace length, must keep 1:4 on self-trace

http://hobi-elektronika.net



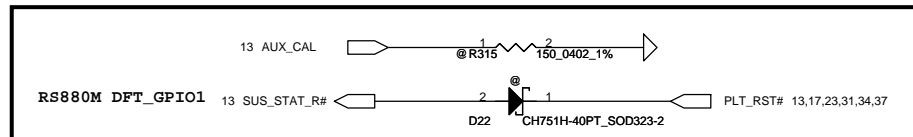


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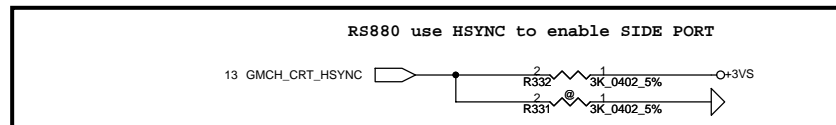
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS880)
0 : Enable (Rs880)



DFT_GPIO1: LOAD_EEPROM_STRAPS

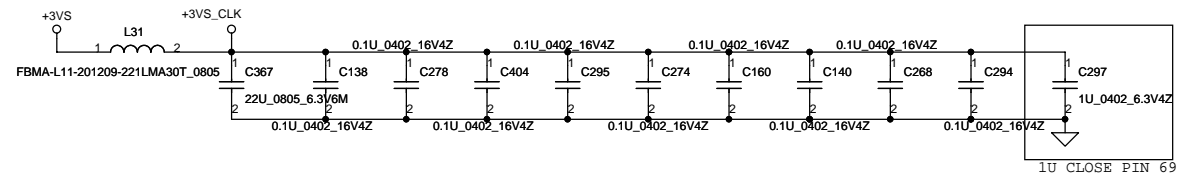
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780/RS880M: DFT_GPIO1 RS880M:SUS_STAT



RS880 use HSYNC to enable SIDE PORT

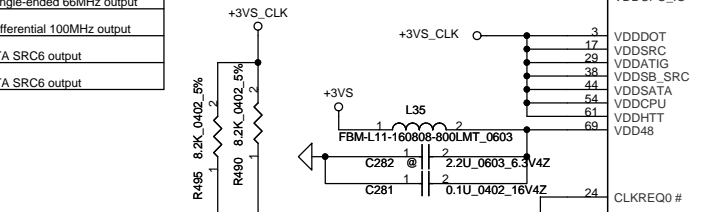
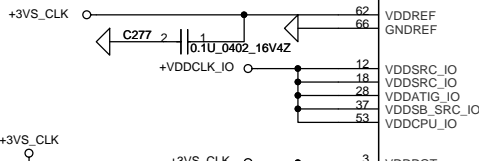
RS740/RS780/RS880M: Enables Side port memory (RS880M use HSYNC#)
0 : Enable (RS880M)
1 : Disable(RS880M)

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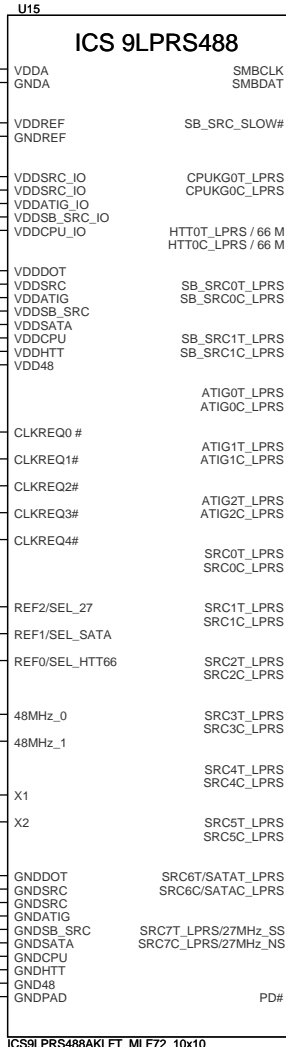


SEL_SATA	1 *	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

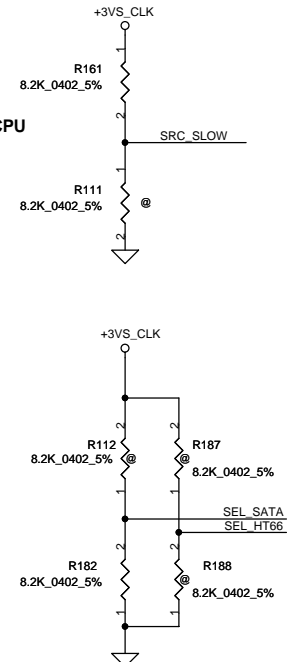
* default



NB CLOCKS	RST740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF



Second--ICS9LPRS488CKLFT-SA000023H10



SRC 0	LAN
SRC 1	
SRC 2	MINI1 (WLAN)
SRC 3	
SRC 4	NB-Alink
SRC 5	
SRC 6	SB-Alink

PCIE LANE REVERSAL

12 PCIE_GTX_C_MRX_P[0..15] ← PCIE GTX C MRX P[0..15]
 12 PCIE_GTX_C_MRX_N[0..15] ← PCIE GTX C MRX N[0..15]
 12 PCIE_MTX_C_GRX_P[0..15] ← PCIE MTX C GRX P[0..15]
 12 PCIE_MTX_C_GRX_N[0..15] ← PCIE MTX C GRX N[0..15]

PCIE_MTX_C_GRX_N15 AE30
 PCIE_MTX_C_GRX_P15 AE31C
 PCIE_MTX_C_GRX_N14 AE29
 PCIE_MTX_C_GRX_P14 AD28C
 PCIE_MTX_C_GRX_N13 AD30
 PCIE_MTX_C_GRX_P13 AC31C
 PCIE_MTX_C_GRX_N12 AC29
 PCIE_MTX_C_GRX_P12 AB28C
 PCIE_MTX_C_GRX_N11 AB30
 PCIE_MTX_C_GRX_P11 AA31C
 PCIE_MTX_C_GRX_N10 AA29
 PCIE_MTX_C_GRX_P10 Y28C
 PCIE_MTX_C_GRX_N9 Y30
 PCIE_MTX_C_GRX_P9 W31C
 PCIE_MTX_C_GRX_N8 W29
 PCIE_MTX_C_GRX_P8 V28C
 PCIE_MTX_C_GRX_N7 V30
 PCIE_MTX_C_GRX_P7 U31C
 PCIE_MTX_C_GRX_N6 U29
 PCIE_MTX_C_GRX_P6 T28C
 PCIE_MTX_C_GRX_N5 T30
 PCIE_MTX_C_GRX_P5 R31C
 PCIE_MTX_C_GRX_N4 R29
 PCIE_MTX_C_GRX_P4 P28C
 PCIE_MTX_C_GRX_N3 P30
 PCIE_MTX_C_GRX_P3 N31C
 PCIE_MTX_C_GRX_N2 N29
 PCIE_MTX_C_GRX_P2 M28C
 PCIE_MTX_C_GRX_N1 M30
 PCIE_MTX_C_GRX_P1 L31C
 PCIE_MTX_C_GRX_N0 L29
 PCIE_MTX_C_GRX_P0 K30C

U88A

PCIE_RX0P
 PCIE_RX0N

PCIE_RX1P
 PCIE_RX1N

PCIE_RX2P
 PCIE_RX2N

PCIE_RX3P
 PCIE_RX3N

PCIE_RX4P
 PCIE_RX4N

PCIE_RX5P
 PCIE_RX5N

PCIE_RX6P
 PCIE_RX6N

PCIE_RX7P
 PCIE_RX7N

PCIE_RX8P
 PCIE_RX8N

PCIE_RX9P
 PCIE_RX9N

PCIE_RX10P
 PCIE_RX10N

PCIE_RX11P
 PCIE_RX11N

PCIE_RX12P
 PCIE_RX12N

PCIE_RX13P
 PCIE_RX13N

PCIE_RX14P
 PCIE_RX14N

PCIE_RX15P
 PCIE_RX15N

PCI EXPRESS INTERFACE

CLOCK

PCIE_REFCLKP
 PCIE_REFCLKN

NC#1
 NC#2
 NC_PWRGOOD

PERSTB

216-0728018 A12 M92-S2 XT FCBGA 0FA

PCIE LANE REVERSAL

PCIE_TX0P AH30 PEG_NRX_C_GTX_N15 C595 1 2 0.1U_0402_16V7K PCIE GTX C MRX N15
 PCIE_TX0N AG31 PEG_NRX_C_GTX_P15 C596 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P15
 PCIE_TX1P AG29 PEG_NRX_C_GTX_N14 C597 1 2 0.1U_0402_16V7K PCIE GTX C MRX N14
 PCIE_TX1N AF28 PEG_NRX_C_GTX_P14 C598 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P14
 PCIE_TX2P AF27 PEG_NRX_C_GTX_N13 C599 1 2 0.1U_0402_16V7K PCIE GTX C MRX N13
 PCIE_TX2N AE26 PEG_NRX_C_GTX_P13 C600 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P13
 PCIE_TX3P AD27 PEG_NRX_C_GTX_N12 C609 1 2 0.1U_0402_16V7K PCIE GTX C MRX N12
 PCIE_TX3N AD26 PEG_NRX_C_GTX_P12 C607 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P12
 PCIE_TX4P AC25 PEG_NRX_C_GTX_N11 C613 1 2 0.1U_0402_16V7K PCIE GTX C MRX N11
 PCIE_TX4N AB25 PEG_NRX_C_GTX_P11 C606 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P11
 PCIE_TX5P Y23 PEG_NRX_C_GTX_N10 C700 1 2 0.1U_0402_16V7K PCIE GTX C MRX N10
 PCIE_TX5N Y24 PEG_NRX_C_GTX_P10 C702 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P10
 PCIE_TX6P AB27 PEG_NRX_C_GTX_N9 C696 1 2 0.1U_0402_16V7K PCIE GTX C MRX N9
 PCIE_TX6N AB26 PEG_NRX_C_GTX_P9 C612 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P9
 PCIE_TX7P Y27 PEG_NRX_C_GTX_N8 C697 1 2 0.1U_0402_16V7K PCIE GTX C MRX N8
 PCIE_TX7N Y26 PEG_NRX_C_GTX_P8 C610 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P8
 PCIE_TX8P W24 PEG_NRX_C_GTX_N7 C611 1 2 0.1U_0402_16V7K PCIE GTX C MRX N7
 PCIE_TX8N W23 PEG_NRX_C_GTX_P7 C643 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P7
 PCIE_TX9P V27 PEG_NRX_C_GTX_N6 C615 1 2 0.1U_0402_16V7K PCIE GTX C MRX N6
 PCIE_TX9N U26 PEG_NRX_C_GTX_P6 C614 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P6
 PCIE_TX10P U24 PEG_NRX_C_GTX_N5 C699 1 2 0.1U_0402_16V7K PCIE GTX C MRX N5
 PCIE_TX10N U23 PEG_NRX_C_GTX_P5 C616 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P5
 PCIE_TX11P T26 PEG_NRX_C_GTX_N4 C617 1 2 0.1U_0402_16V7K PCIE GTX C MRX N4
 PCIE_TX11N T27 PEG_NRX_C_GTX_P4 C618 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P4
 PCIE_TX12P T24 PEG_NRX_C_GTX_N3 C622 1 2 0.1U_0402_16V7K PCIE GTX C MRX N3
 PCIE_TX12N T23 PEG_NRX_C_GTX_P3 C626 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P3
 PCIE_TX13P P27 PEG_NRX_C_GTX_N2 C701 1 2 0.1U_0402_16V7K PCIE GTX C MRX N2
 PCIE_TX13N P26 PEG_NRX_C_GTX_P2 C639 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P2
 PCIE_TX14P P24 PEG_NRX_C_GTX_N1 C640 1 2 0.1U_0402_16V7K PCIE GTX C MRX N1
 PCIE_TX14N P23 PEG_NRX_C_GTX_P1 C628 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P1
 PCIE_TX15P M27 PEG_NRX_C_GTX_N0 C698 1 2 0.1U_0402_16V7K PCIE GTX C MRX N0
 PCIE_TX15N M26 PEG_NRX_C_GTX_P0 C644 1 1 2 0.1U_0402_16V7K PCIE GTX C MRX P0

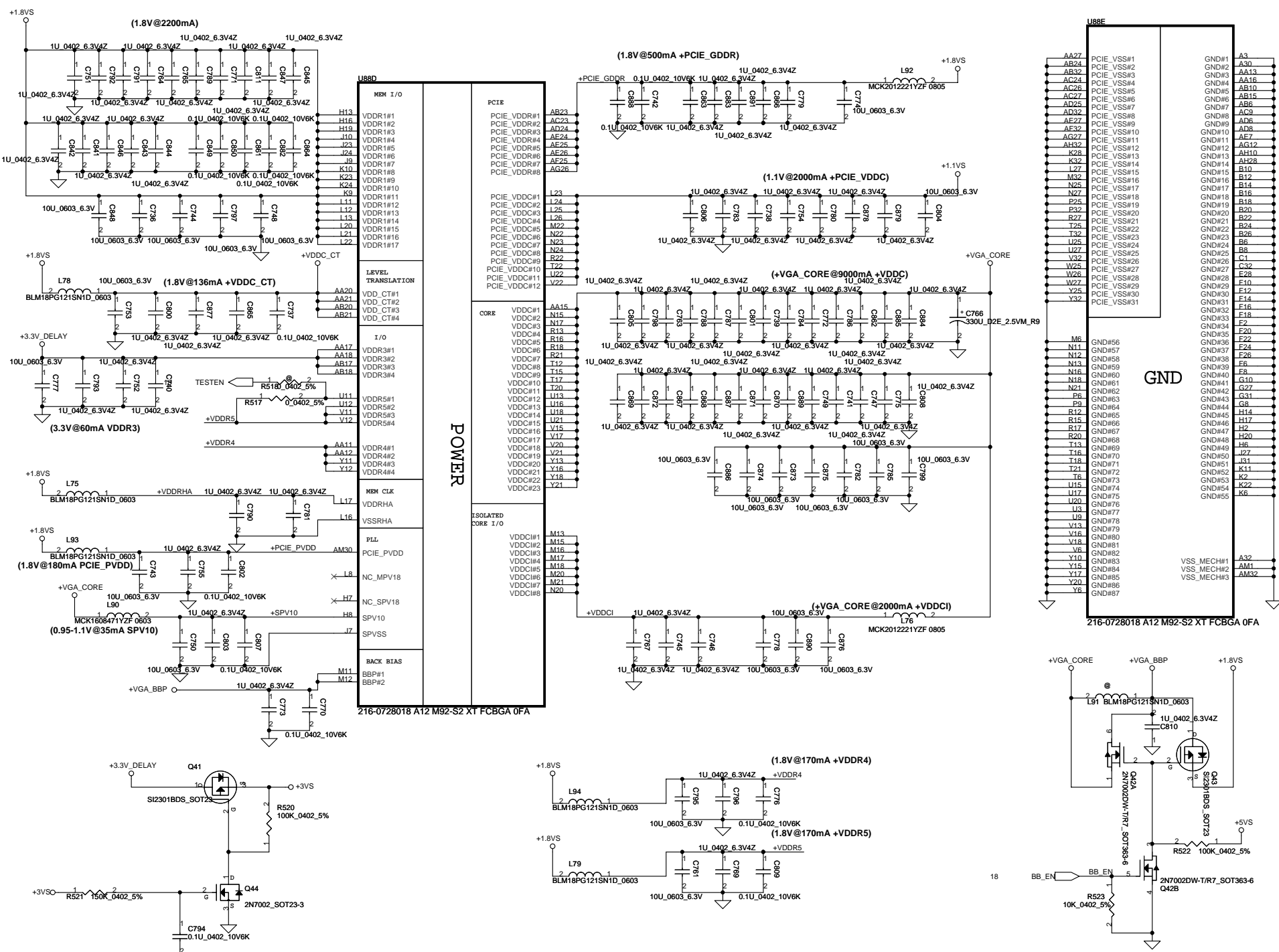
CALIBRATION

PCIE_CALRP
 PCIE_CALRN

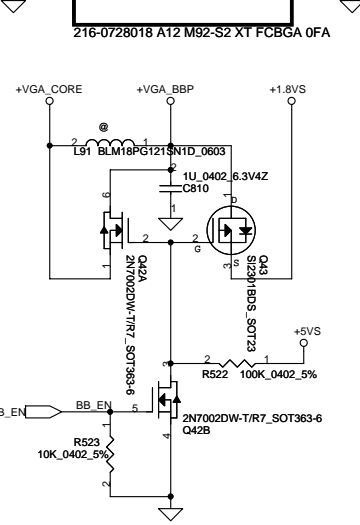
Y22 R467 1 2 1.27K_0402_1%
 AA22 R469 1 2 2K_0402_1% +1.1VS

16 CLK_PCIE_VGA# CLK_PCIE_VGA# AK30
 16 CLK_PCIE_VGA# CLK_PCIE_VGA# AK32C
 For Future ASIC Pin N10 need pull down
 @ 10K_0402_5%
 R468 1 2
 13,15,23,31,34,37 PLT_RST# 2 R578 1 0.0402_5%
 AL27C
 @ C645 1 2 10P_0402_50V8J
 For ESD Request

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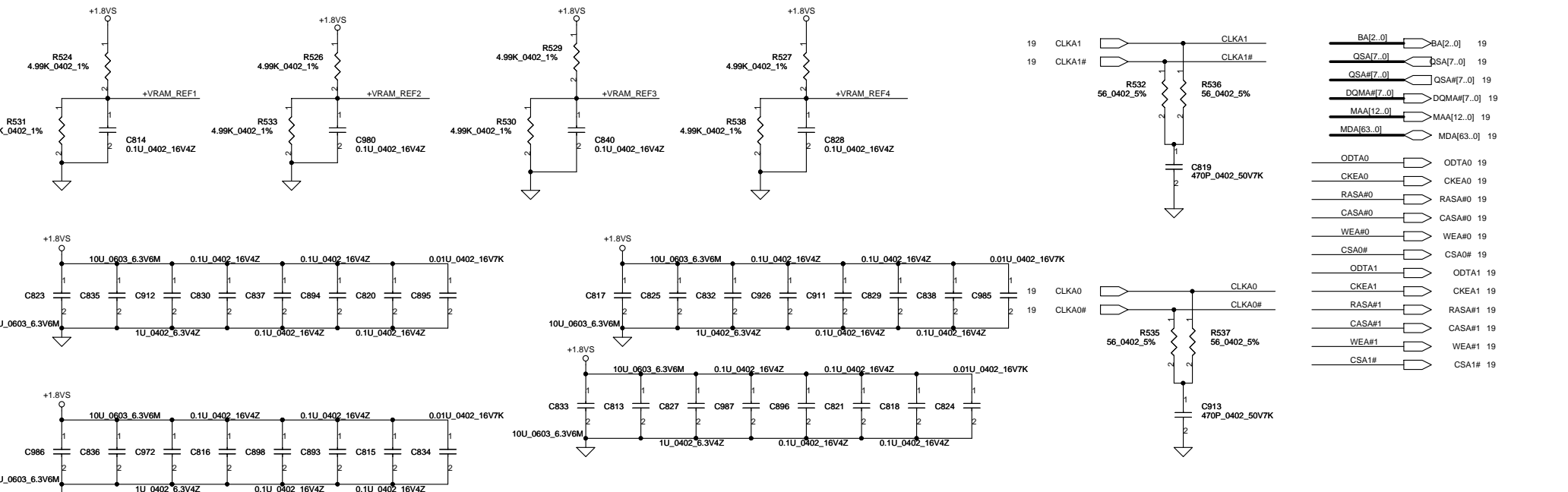
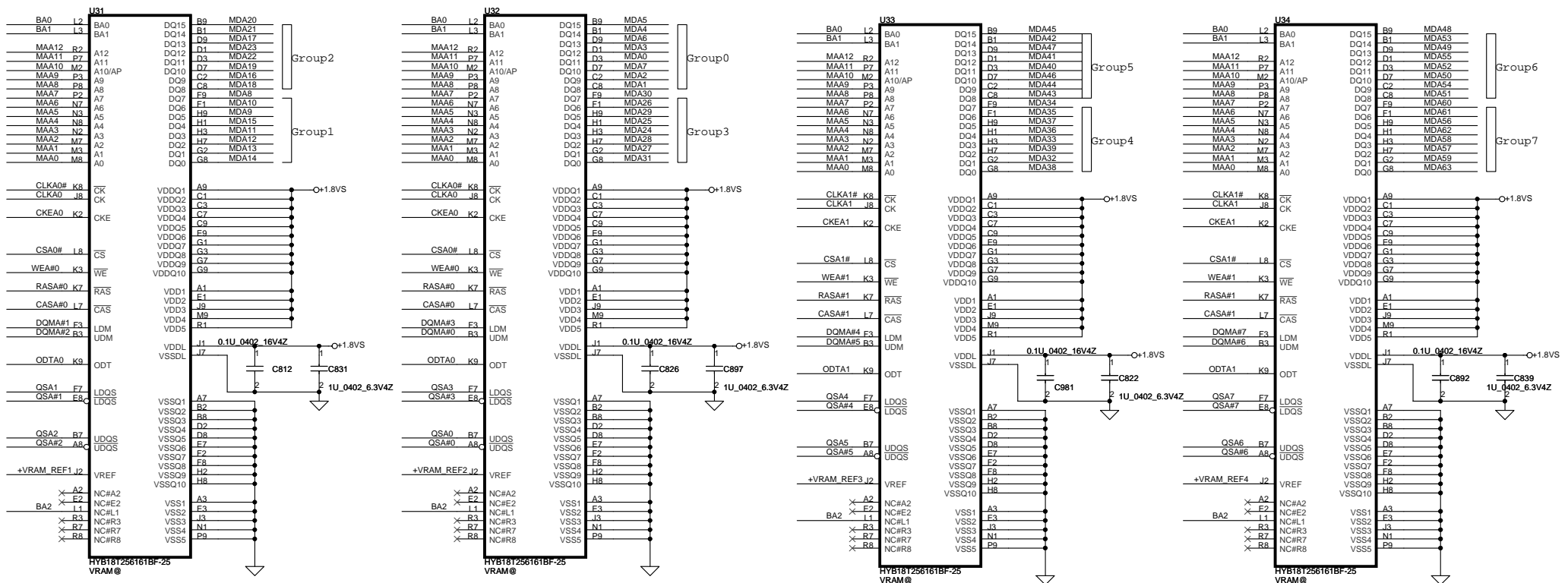


U88E	
AA27	PCIE_VSS#1
AB24	PCIE_VSS#2
AB32	PCIE_VSS#3
AC24	PCIE_VSS#4
AC26	PCIE_VSS#5
AC27	PCIE_VSS#6
AD25	PCIE_VSS#7
AD32	PCIE_VSS#8
AE27	PCIE_VSS#9
AF32	PCIE_VSS#10
AG27	PCIE_VSS#11
AG32	PCIE_VSS#12
K28	PCIE_VSS#13
K32	PCIE_VSS#14
L27	PCIE_VSS#15
M32	PCIE_VSS#16
N25	PCIE_VSS#17
N27	PCIE_VSS#18
P25	PCIE_VSS#19
P32	PCIE_VSS#20
R27	PCIE_VSS#21
T25	PCIE_VSS#22
T32	PCIE_VSS#23
U25	PCIE_VSS#24
U27	PCIE_VSS#25
V32	PCIE_VSS#26
W25	PCIE_VSS#27
W26	PCIE_VSS#28
W27	PCIE_VSS#29
Y25	PCIE_VSS#30
Y32	PCIE_VSS#31
GND	
M6	GND#56
N11	GND#57
N12	GND#58
N13	GND#59
N16	GND#60
N18	GND#61
N21	GND#62
P6	GND#63
P9	GND#64
R12	GND#65
R15	GND#66
R17	GND#67
R20	GND#68
T13	GND#69
T16	GND#70
T18	GND#71
T21	GND#72
T6	GND#73
U15	GND#74
U17	GND#75
U20	GND#76
U3	GND#77
U9	GND#78
V13	GND#79
V16	GND#80
V18	GND#81
V6	GND#82
Y10	GND#83
Y15	GND#84
Y17	GND#85
Y6	GND#86
Y8	GND#87
A30	GND#1
AA13	GND#2
AA16	GND#3
AB10	GND#4
AB15	GND#5
AB8	GND#6
AC2	GND#7
AD6	GND#8
AD8	GND#9
AE7	GND#10
AG12	GND#11
AH10	GND#12
AH28	GND#13
B10	GND#14
B12	GND#15
B14	GND#16
B16	GND#17
B18	GND#18
B20	GND#19
B22	GND#20
B24	GND#21
B26	GND#22
B8	GND#23
C8	GND#24
C1	GND#25
C32	GND#26
E28	GND#27
F10	GND#28
F12	GND#29
F14	GND#30
F16	GND#31
F2	GND#32
F20	GND#33
F22	GND#34
F24	GND#35
F26	GND#36
F8	GND#37
G10	GND#38
G12	GND#39
G31	GND#40
G8	GND#41
H14	GND#42
H17	GND#43
H2	GND#44
H20	GND#45
H6	GND#46
J31	GND#47
K11	GND#48
K2	GND#49
K22	GND#50
K6	GND#51
A32	VSS_MECH#1
AM1	VSS_MECH#2
AM32	VSS_MECH#3



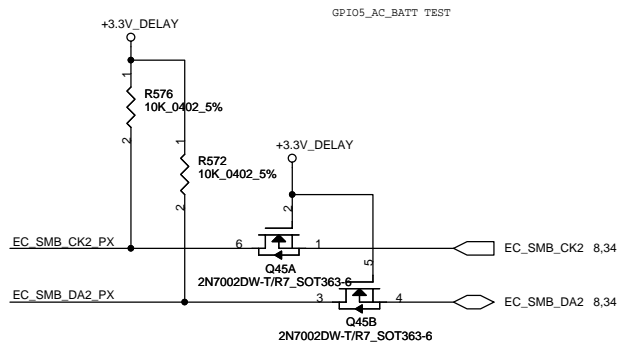
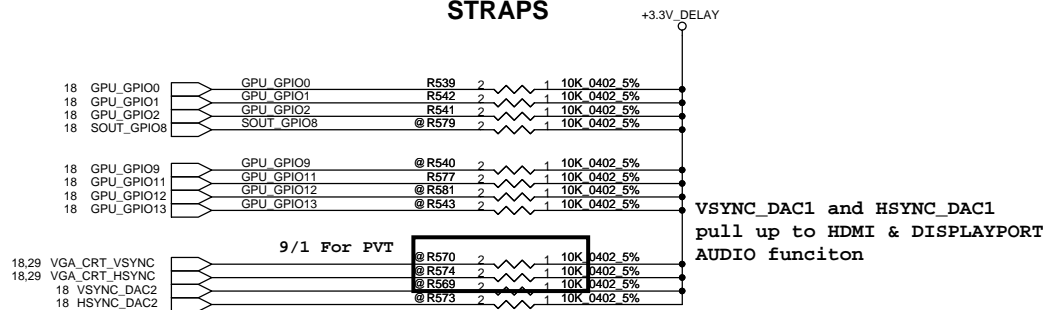
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<http://hobi-elektronika.net>

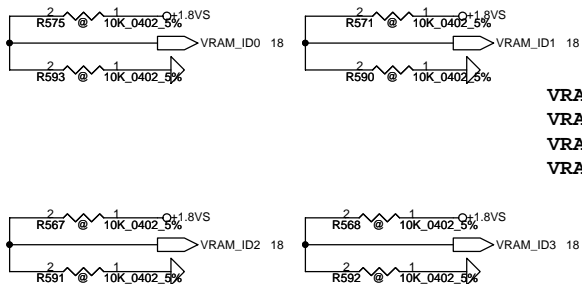
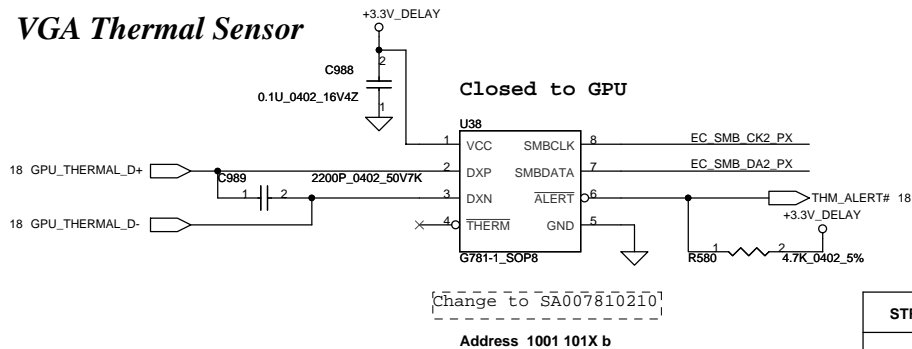


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STRAPS



VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMIDCFG(2:0)	GPIO[13:11]	BIF_RX_PLL_CALIB_BP	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HARD	H2SYNC	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

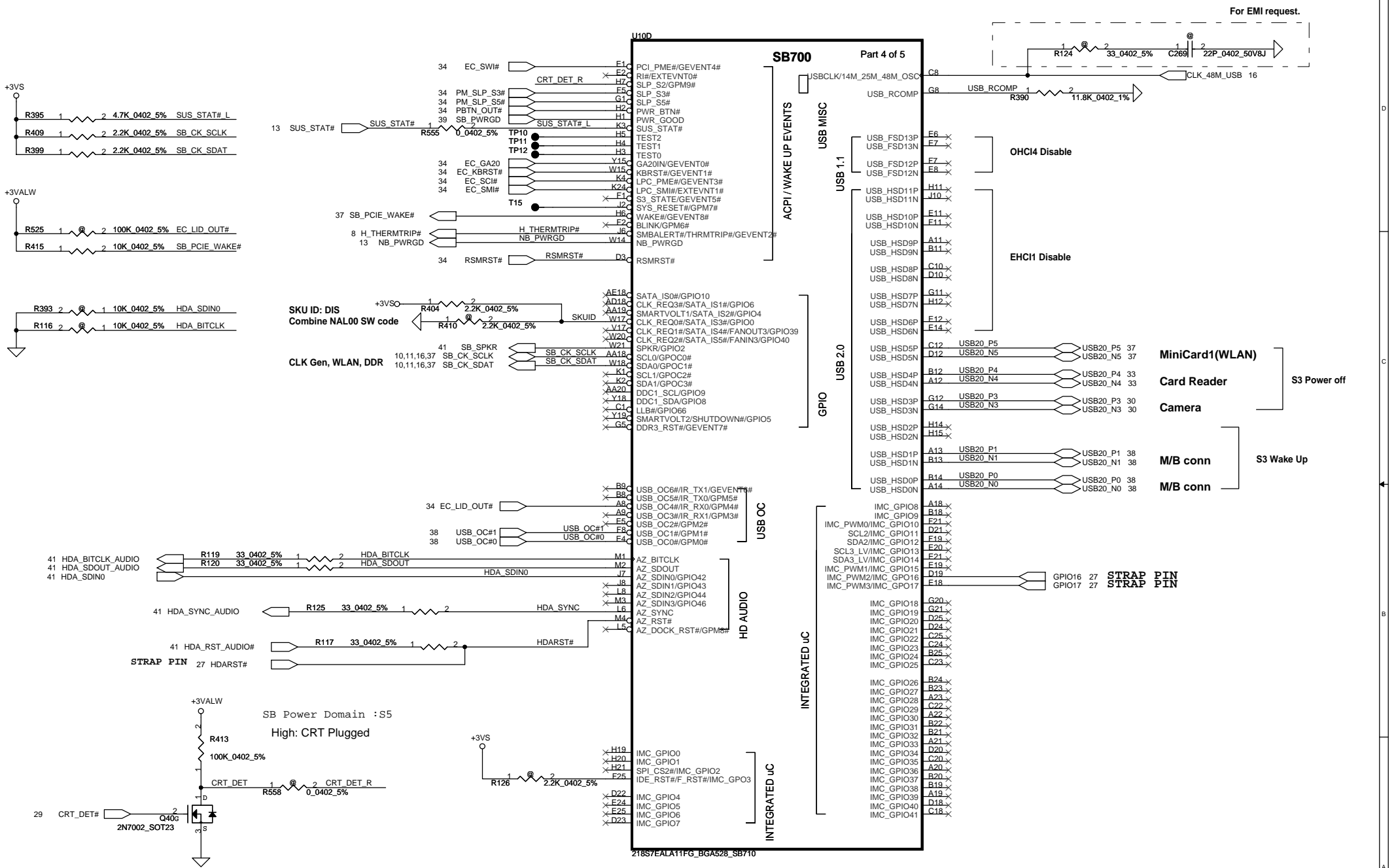
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPIO_28_TDO	GPIO21_BB_EN

[illegible]

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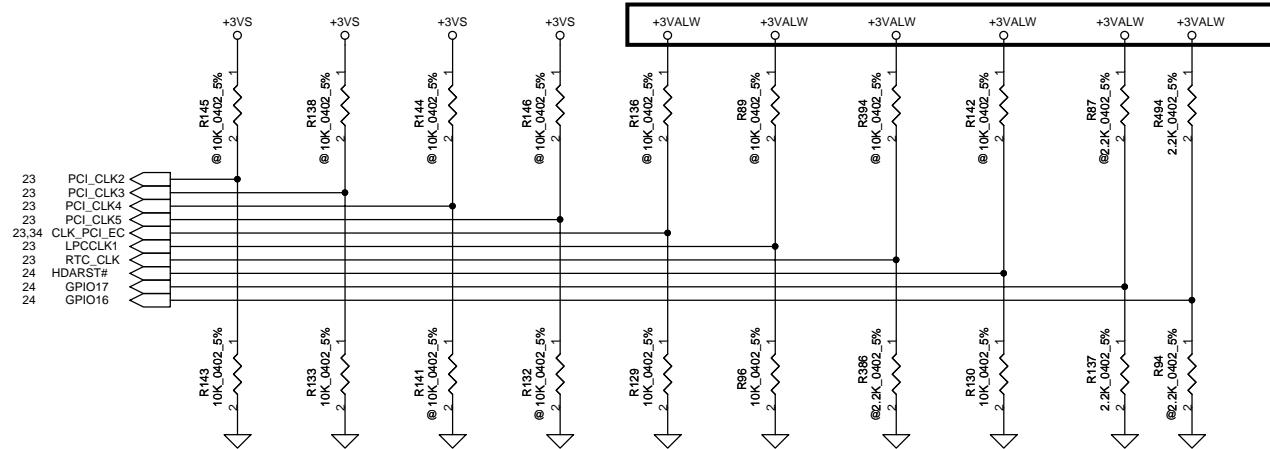


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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

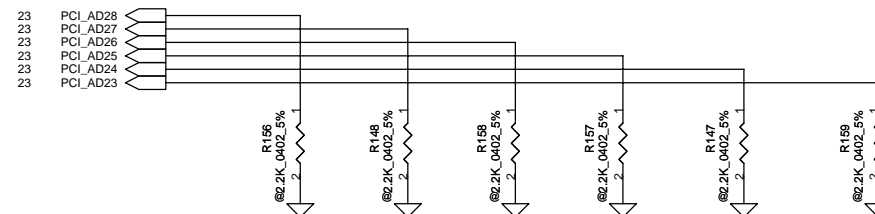
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



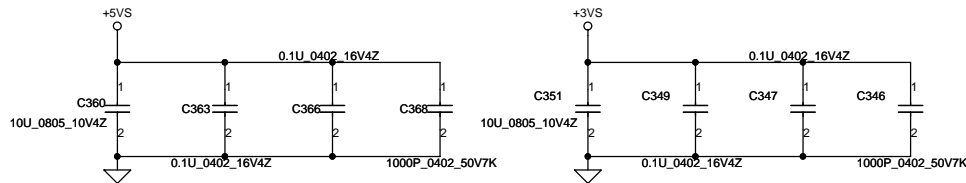
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

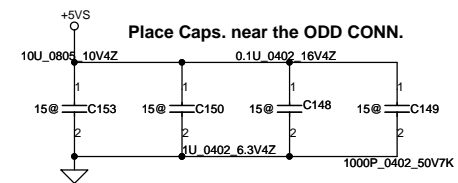
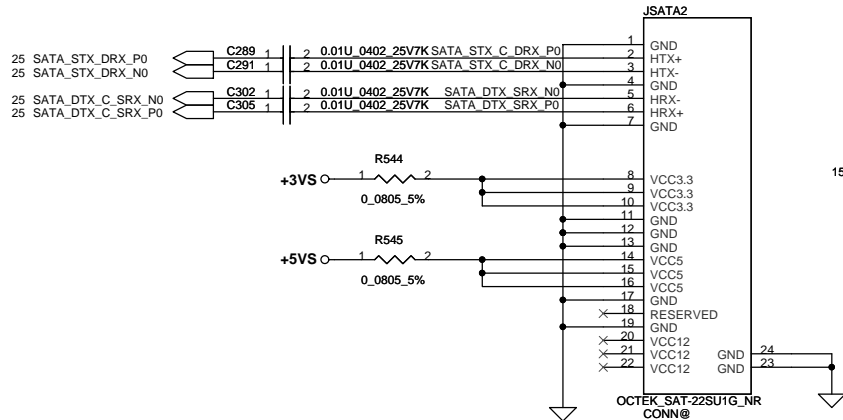
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



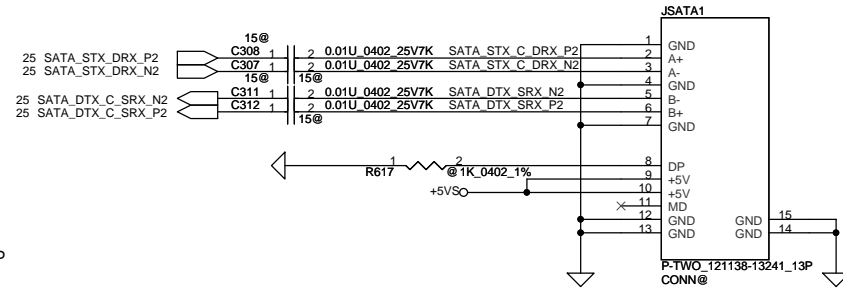
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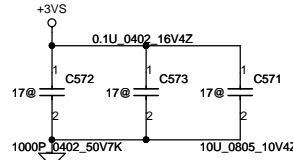
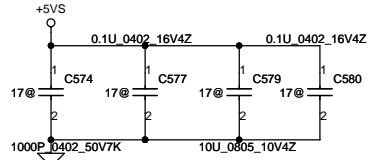
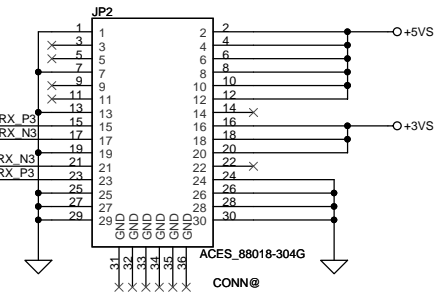
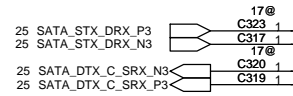
SATA HDD CONN



SATA ODD CONN

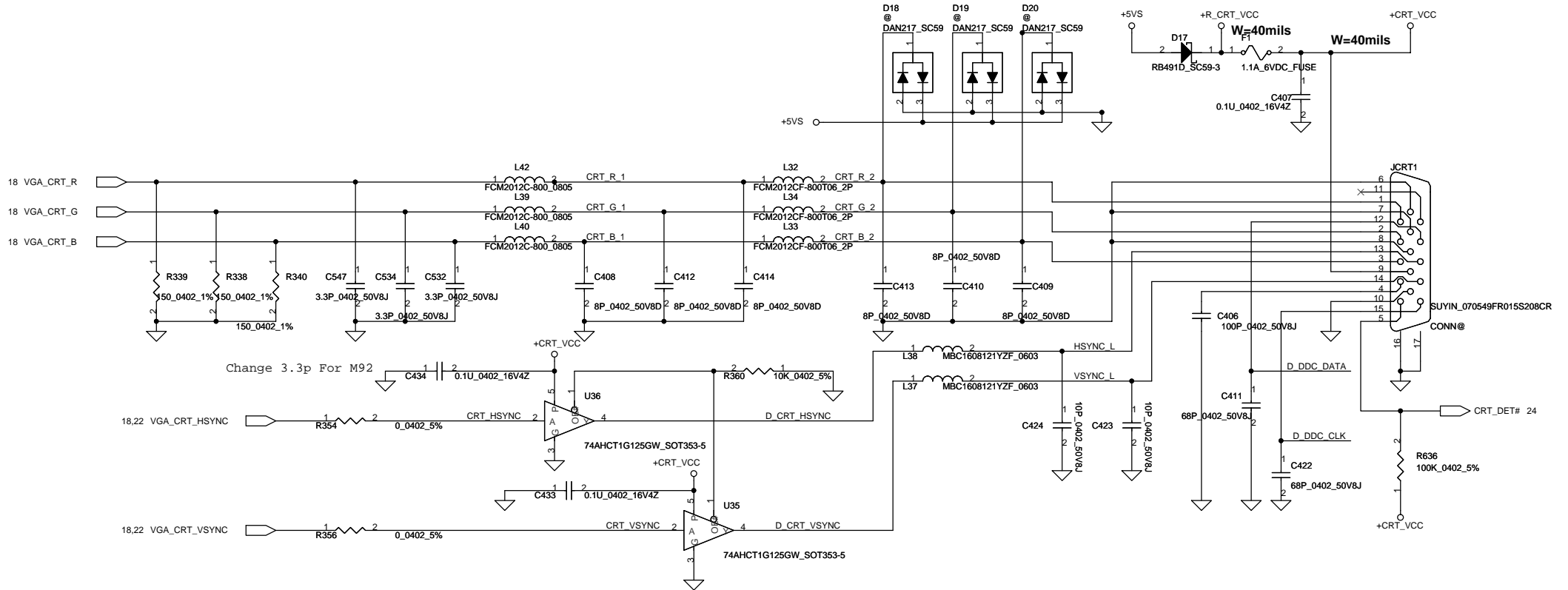


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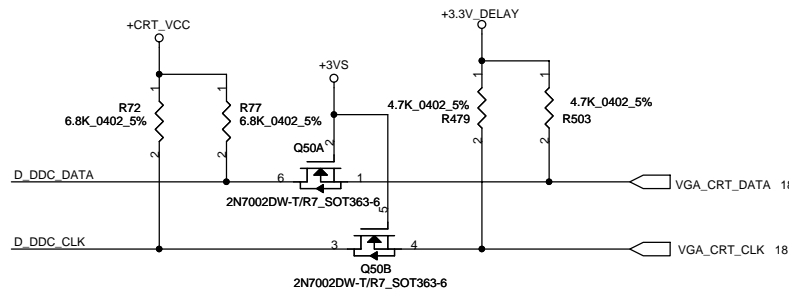


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CRT Connector

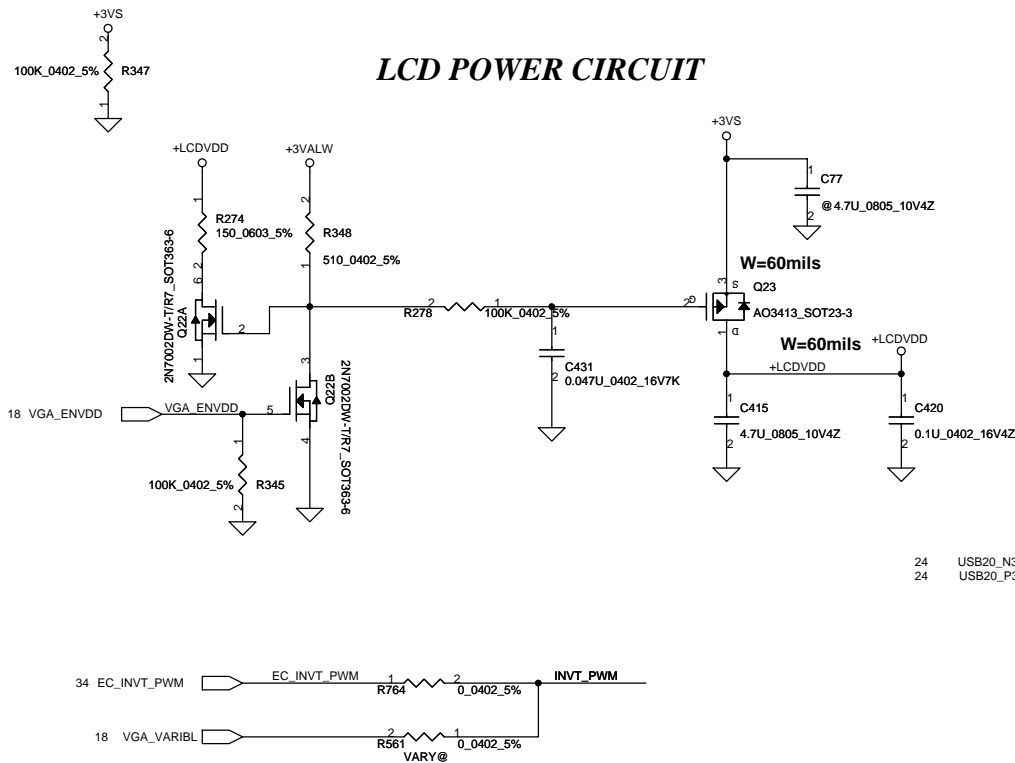


Close to Conn side

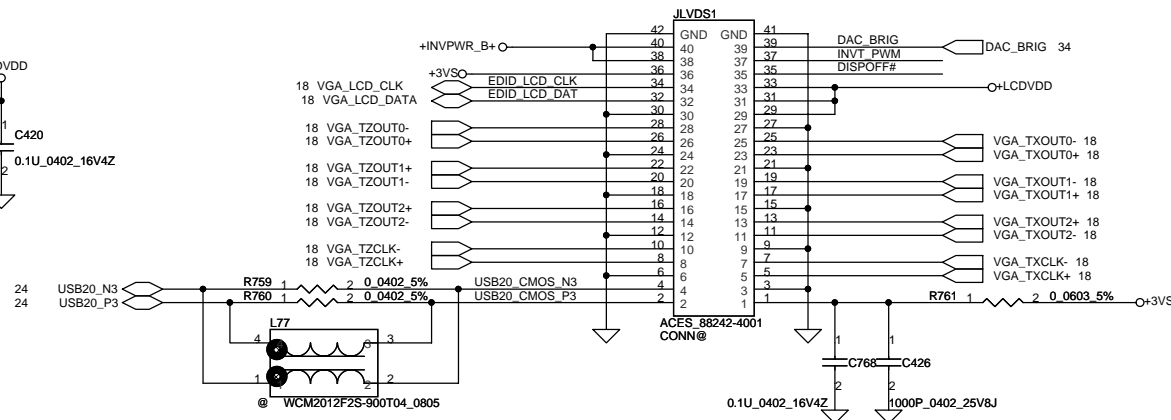


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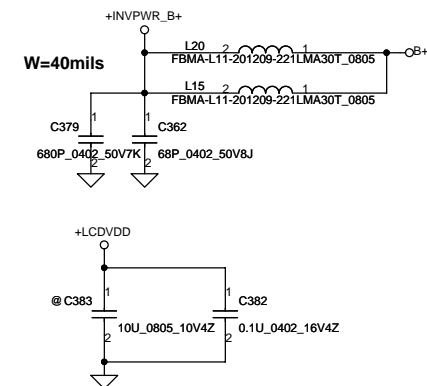
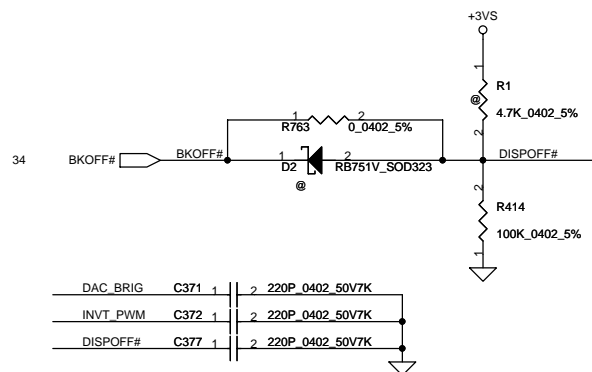
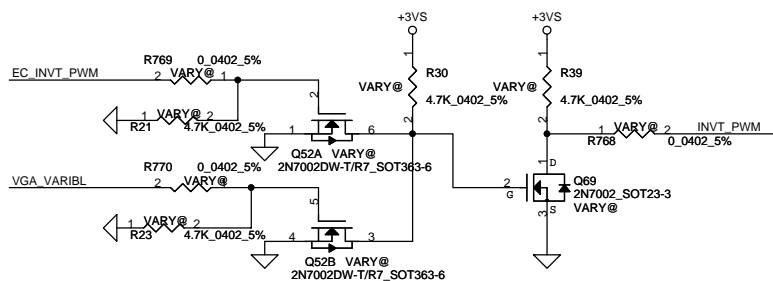
LCD POWER CIRCUIT



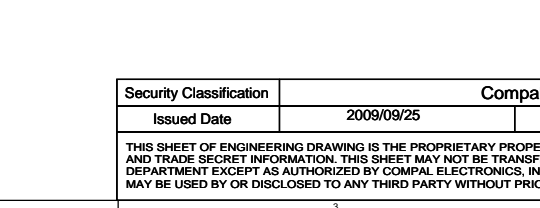
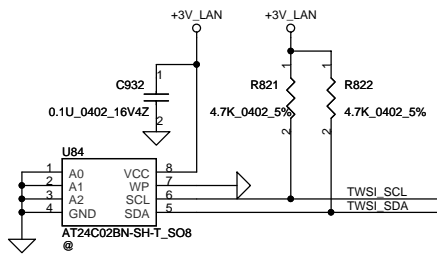
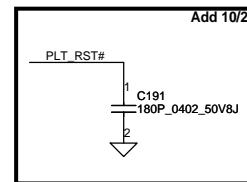
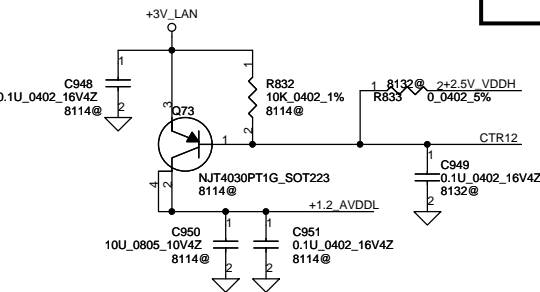
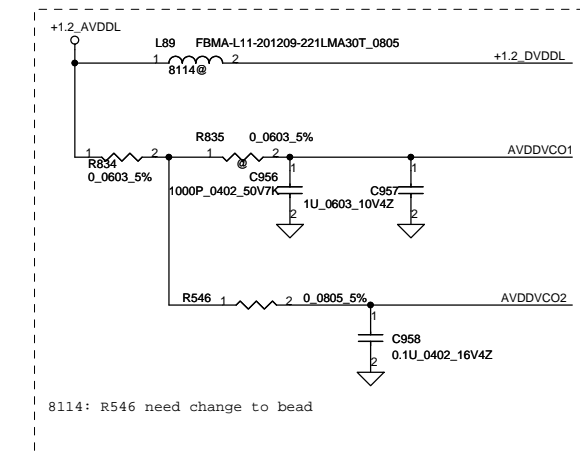
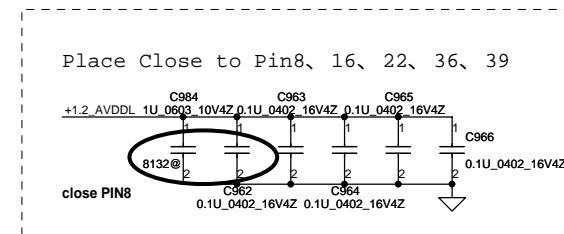
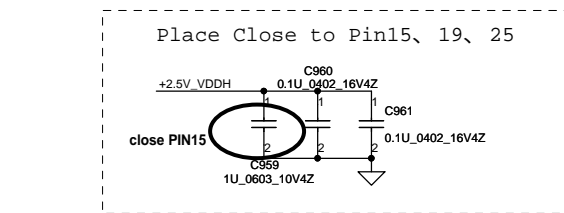
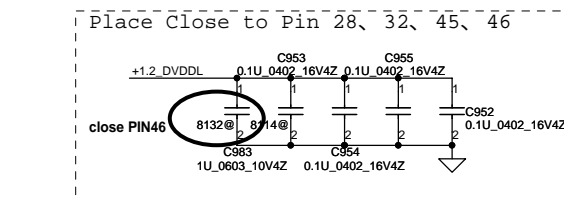
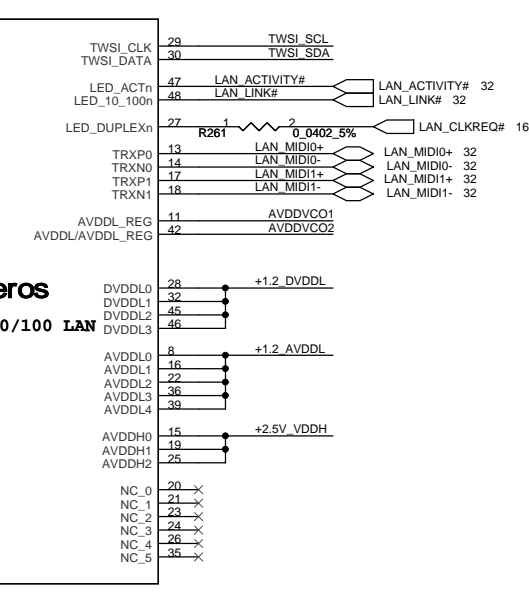
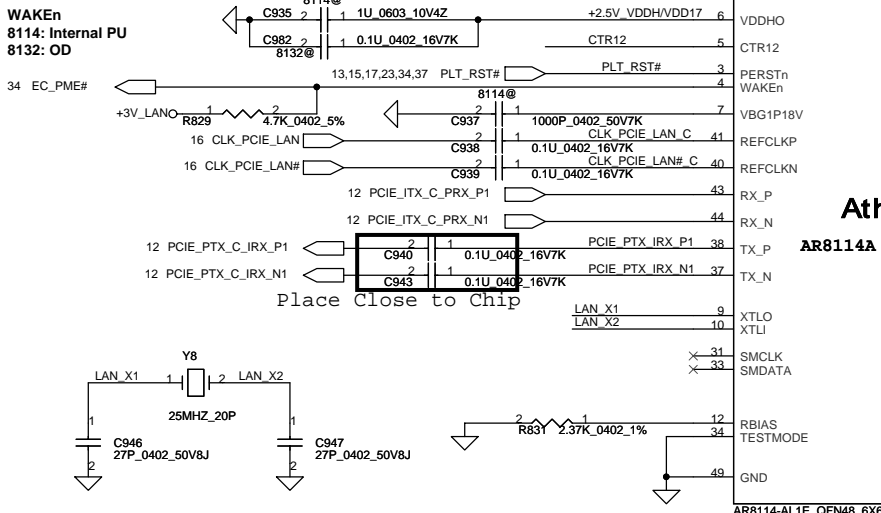
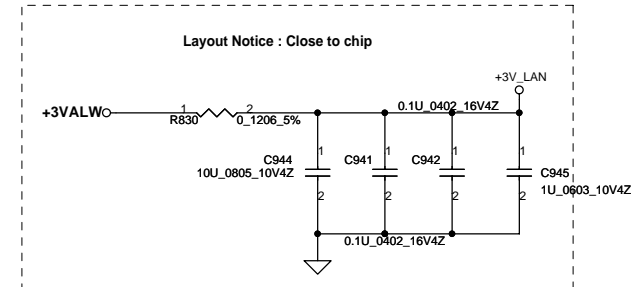
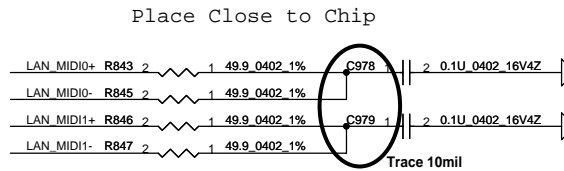
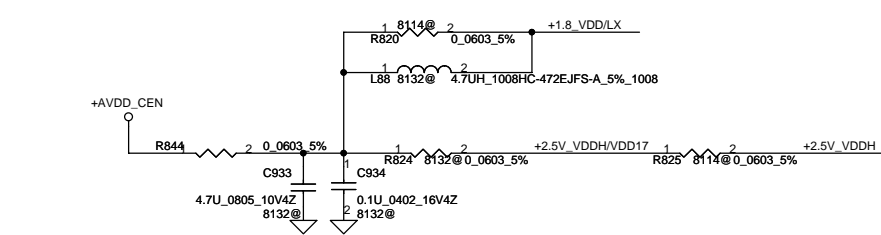
LCD/PANEL CONN.



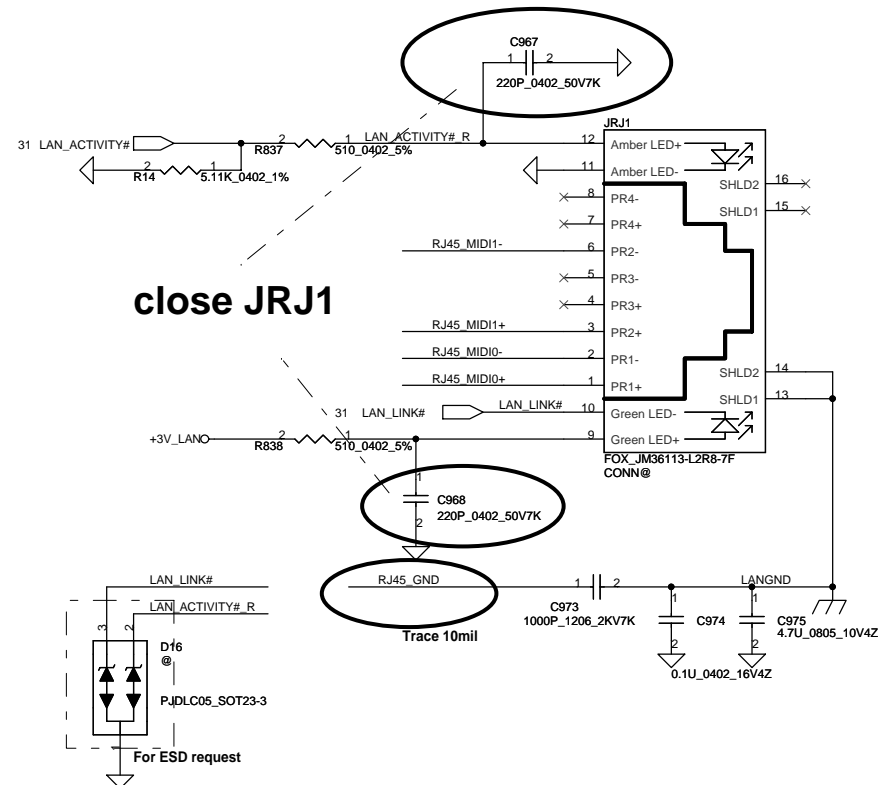
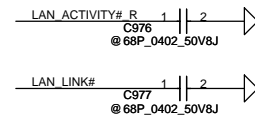
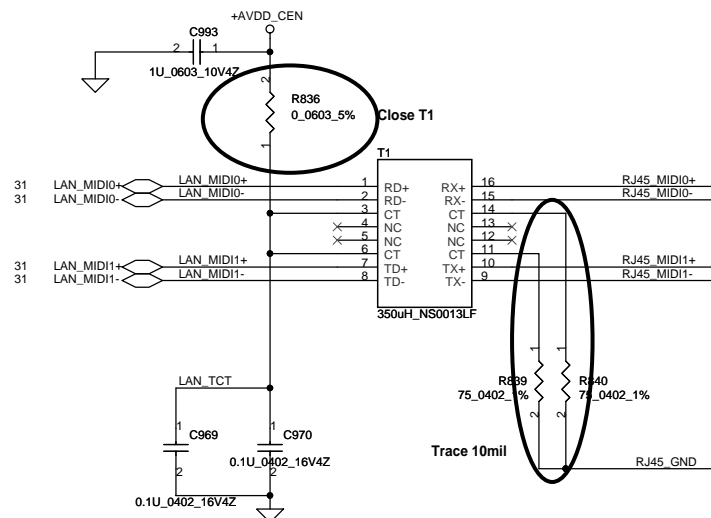
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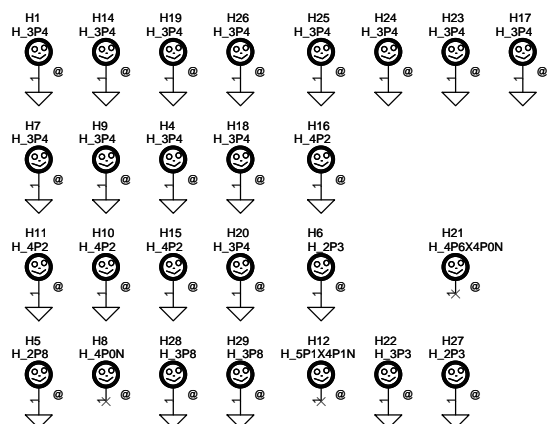
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								SCHEMATIC MB A5992		
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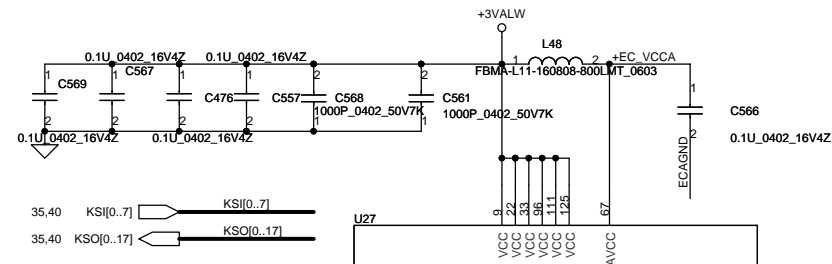
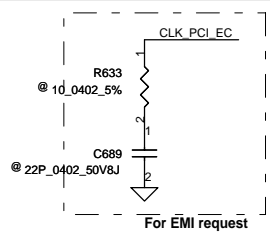
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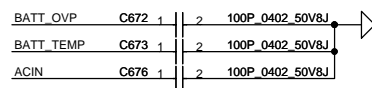
PCB Federal Mark PAD



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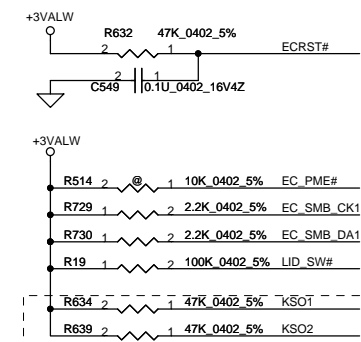
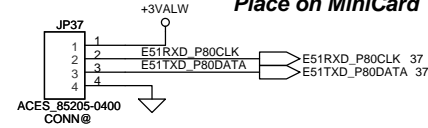


Please close to EC pin

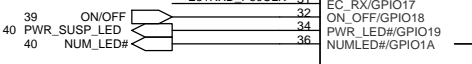
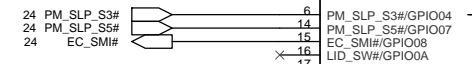
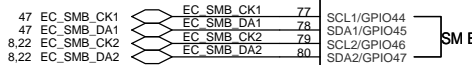
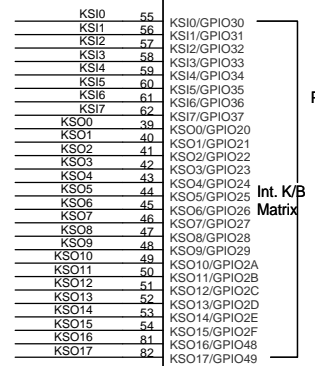
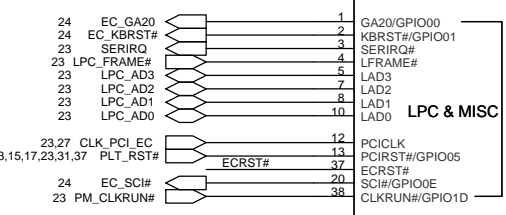
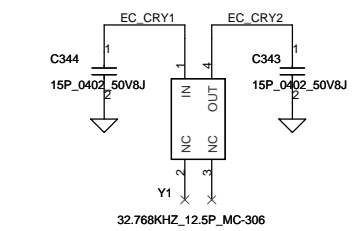
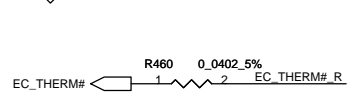
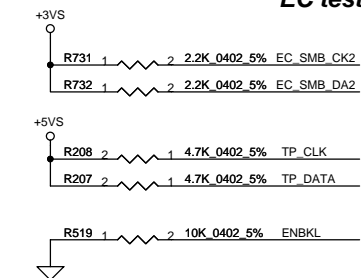


For EC Tools

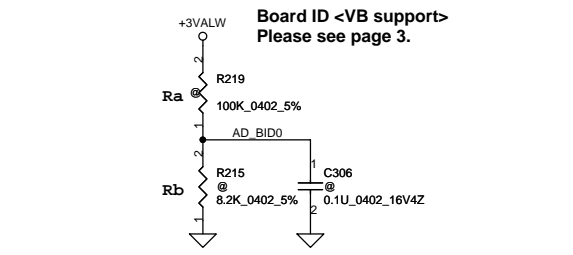
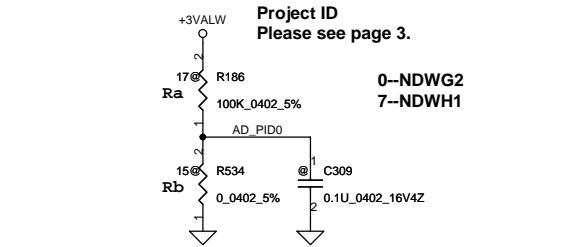
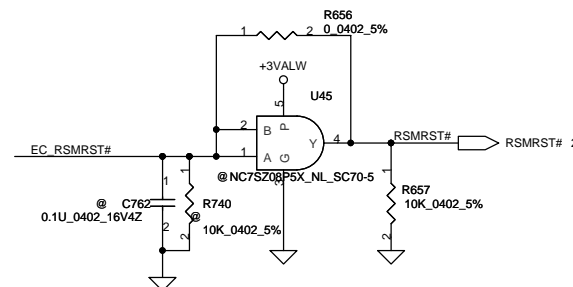
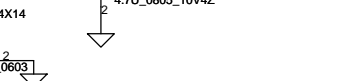
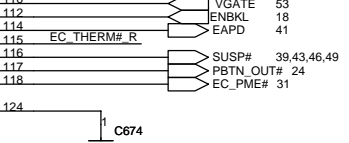
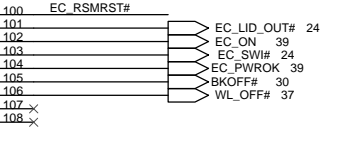
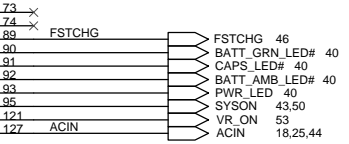
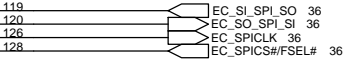
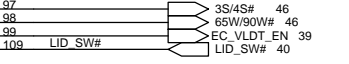
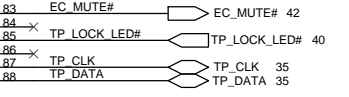
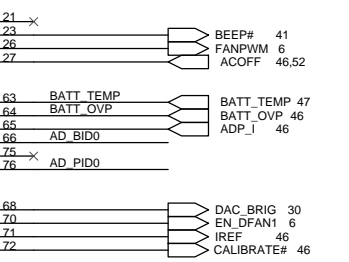
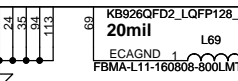
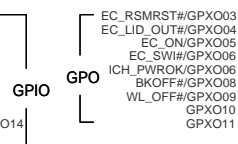
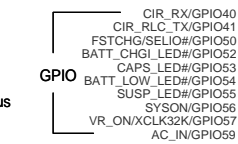
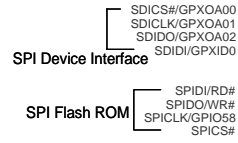
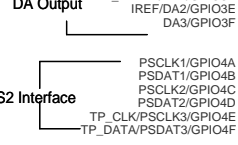
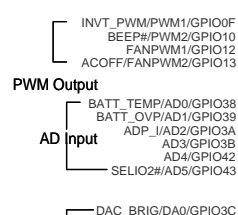
Place on MiniCard



EC test-mode issue



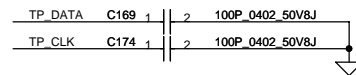
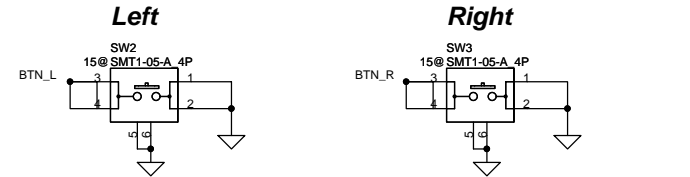
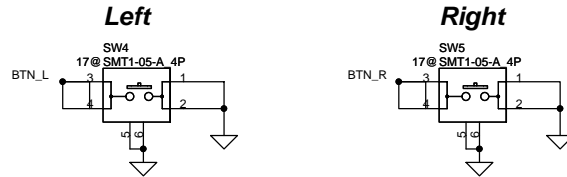
Chagne to D3 version



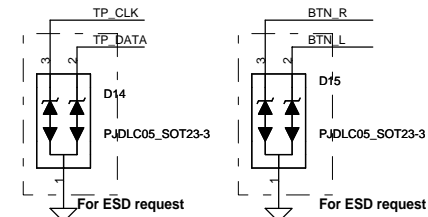
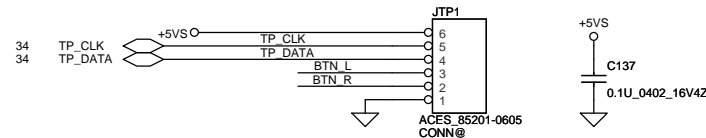
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For 17"

For 15"



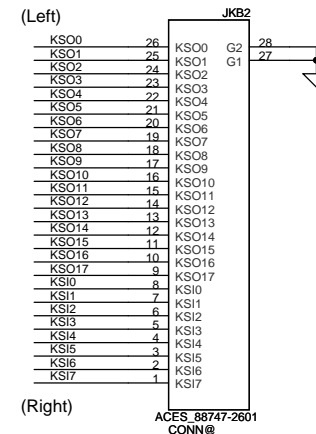
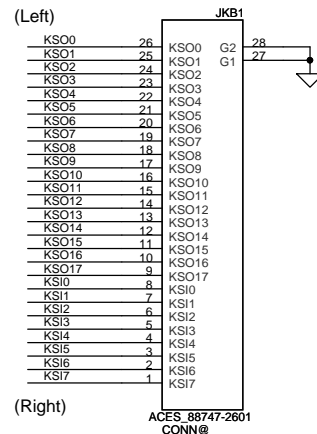
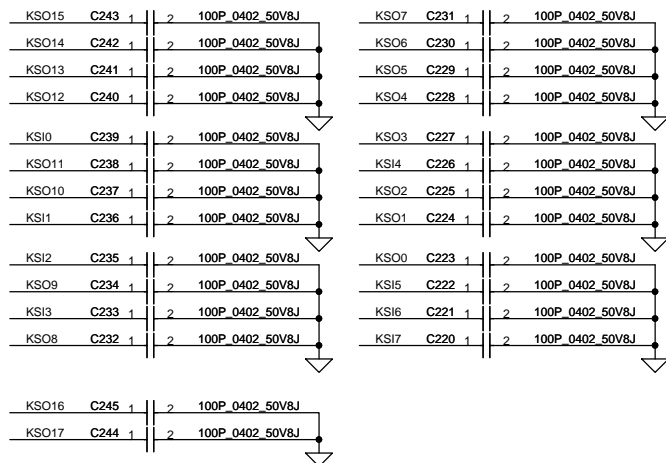
TP/B Conn.



Change to SCA00000200

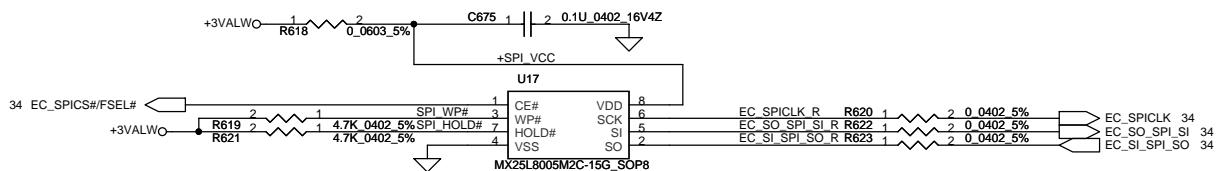
INT_KBD Conn.

KB1 for 15"
KB2 for 17"



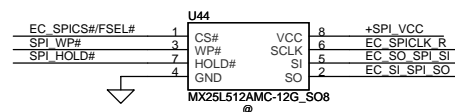
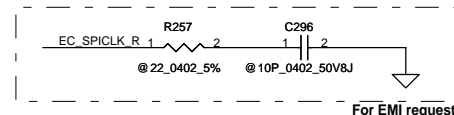
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SPI Flash ROM 16M*1



SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

ONLY MXIC used in this project (66MHz)

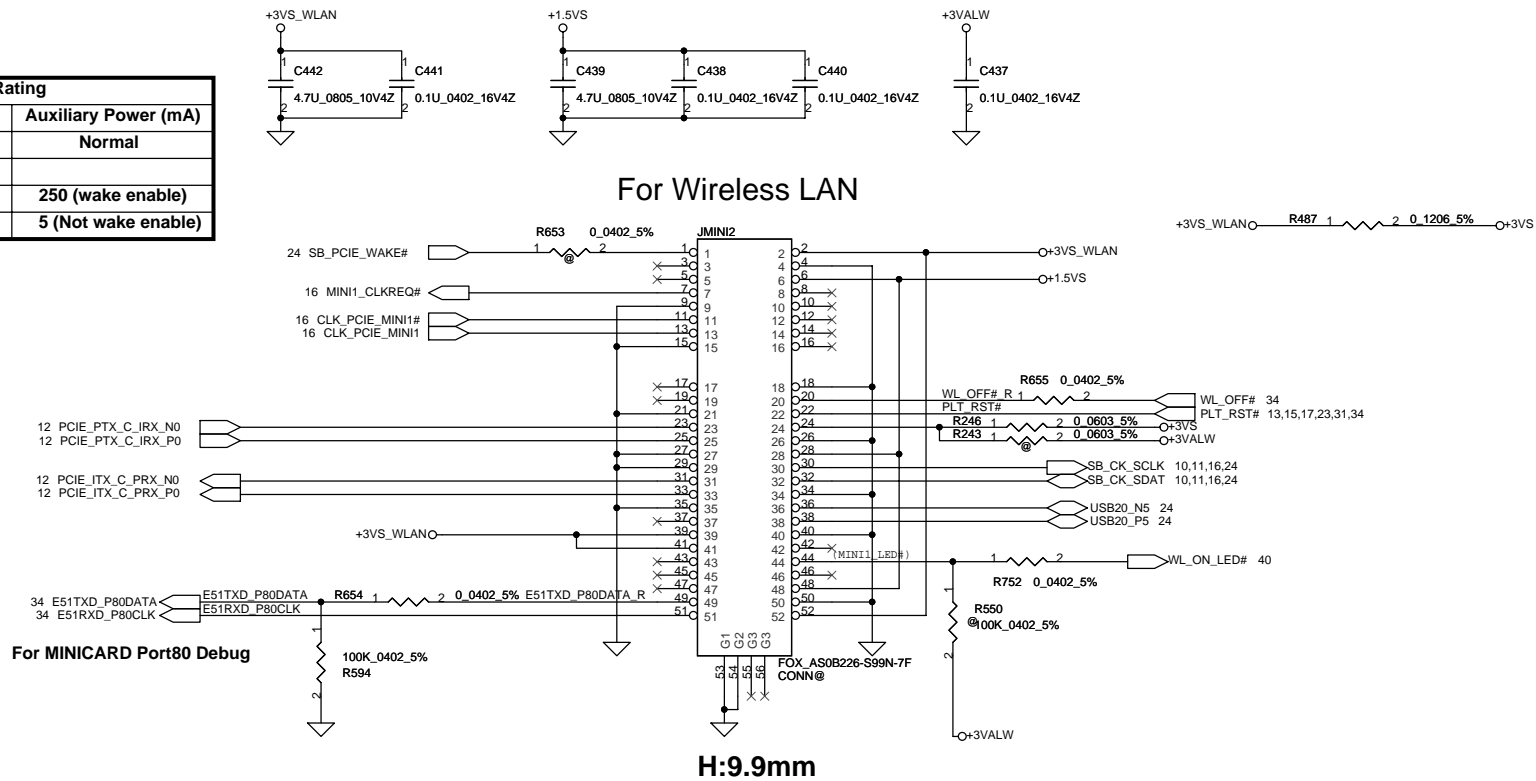


Reserved for BIOS simulator.
 Footprint SO8

SPI ROM Footprint 150mil

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				Date: Thursday, March 18, 2010	Sheet 36 of 55	

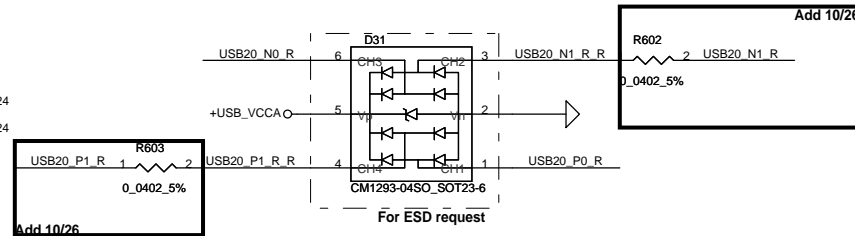
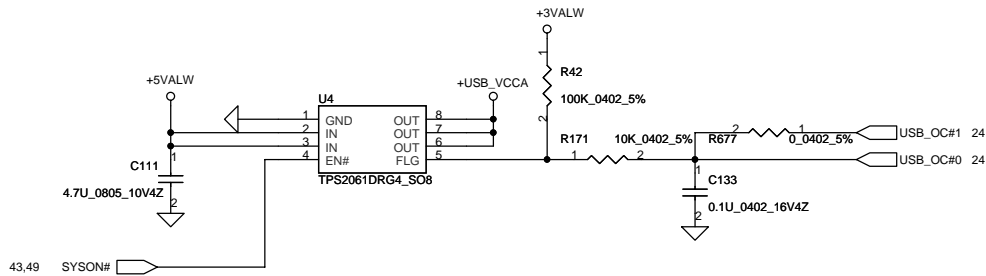
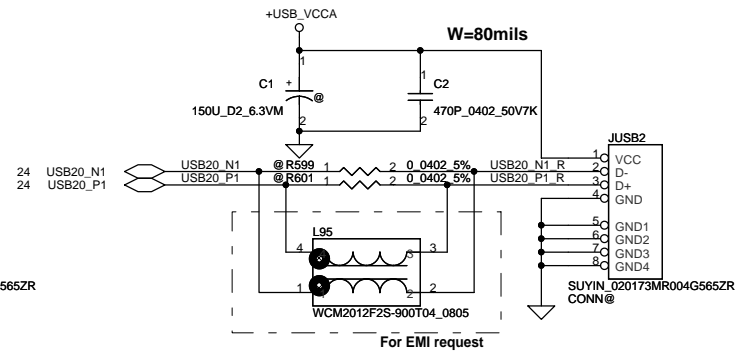
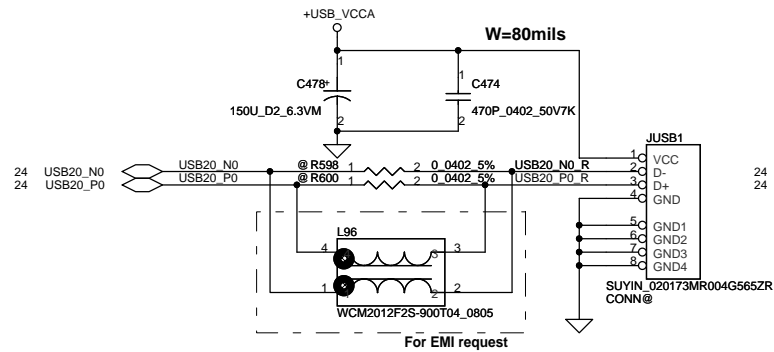
Mini Card Power Rating			
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	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



H:9.9mm

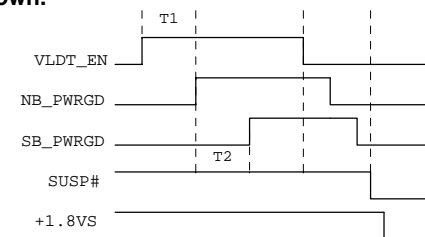
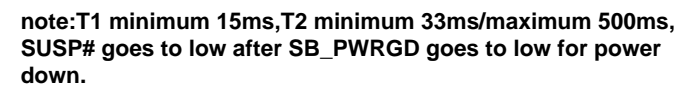
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USB CONN. 1 & 2



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For South Bridge

[illegible]

Power Button

TOP Side

Bottom Side

40 ON/OFFBTN#

ON/OFFBTN#

1

2

1

R765 10K_0603_5%

R766 10K_0603_5%

D10

DAN202UT106_SCT0-3

2

3

51ON#

ON/OFF

34

44

51ON#

44

34

EC_ON

EC_ON

2

1

R290 10K_0402_5%

Q17

2N7002_SOT23

2

1

C358 1000P_0402_50V7K

D11

RLZ20A_LL34

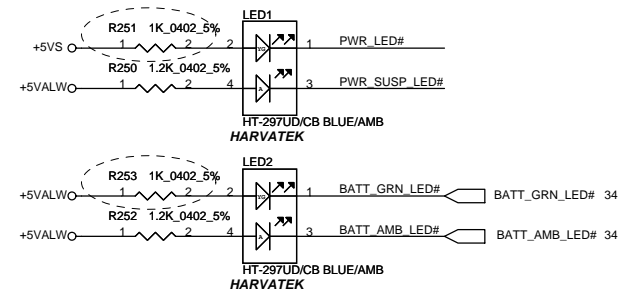
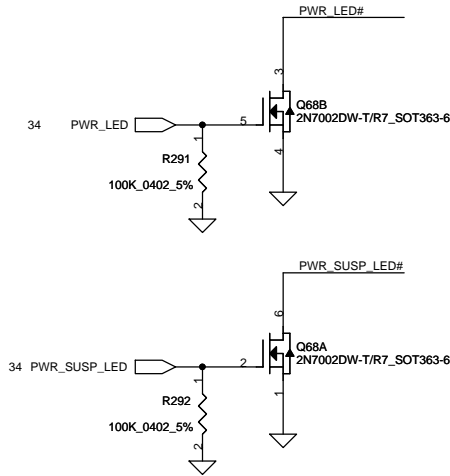
SW10

SMT1-05-A 4P

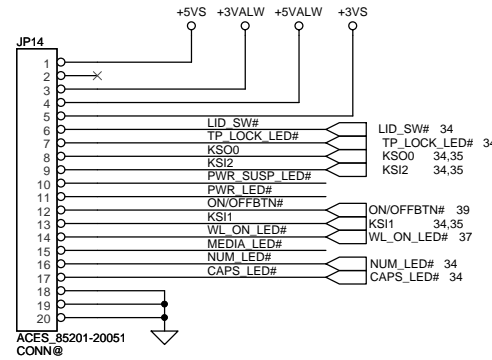
ON/OFFBTN#

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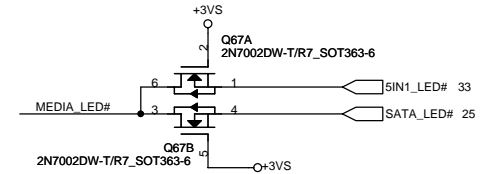
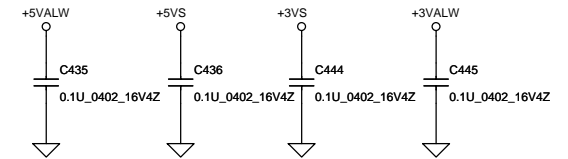
To PWR LED/B



BLUE/AMB LED

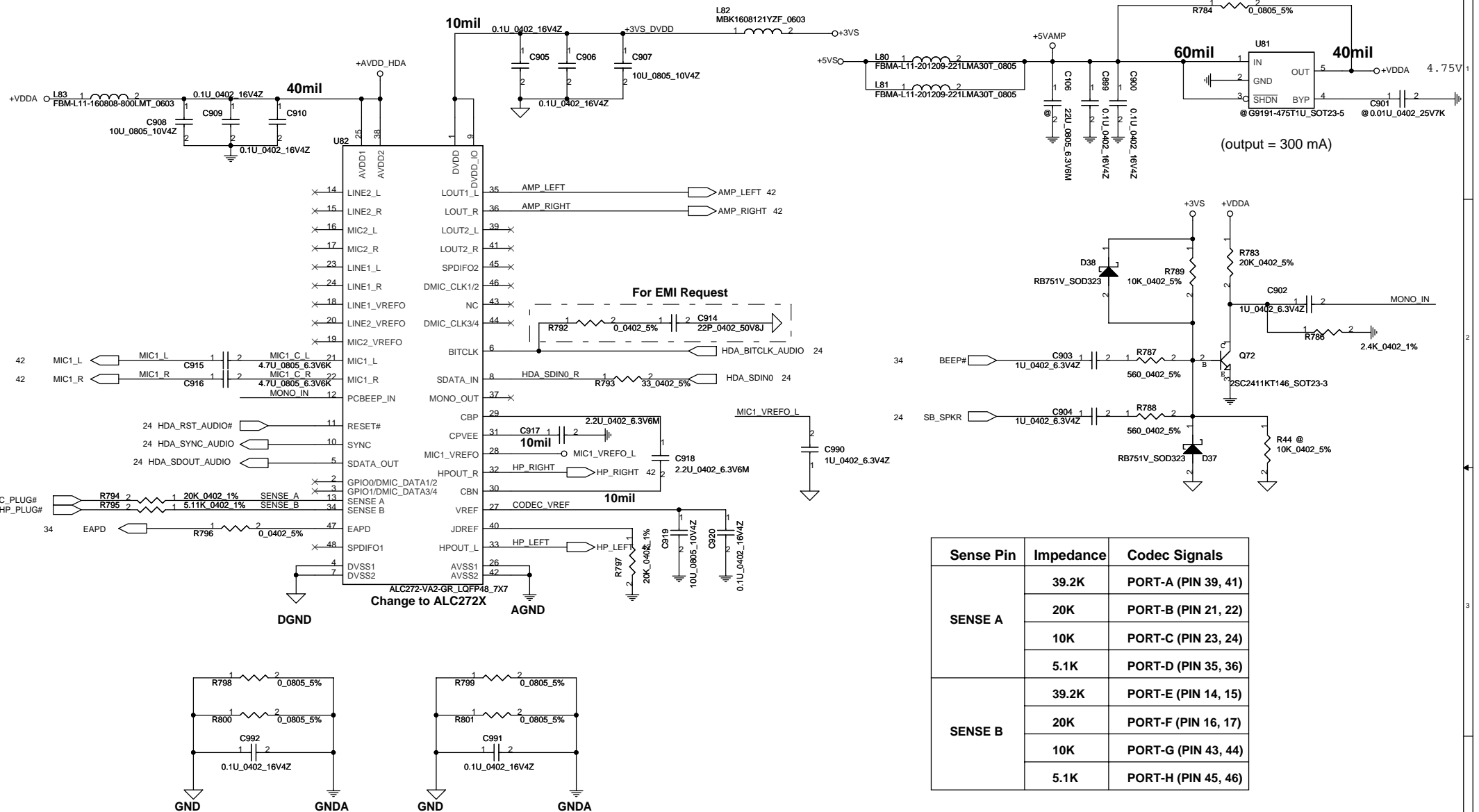


	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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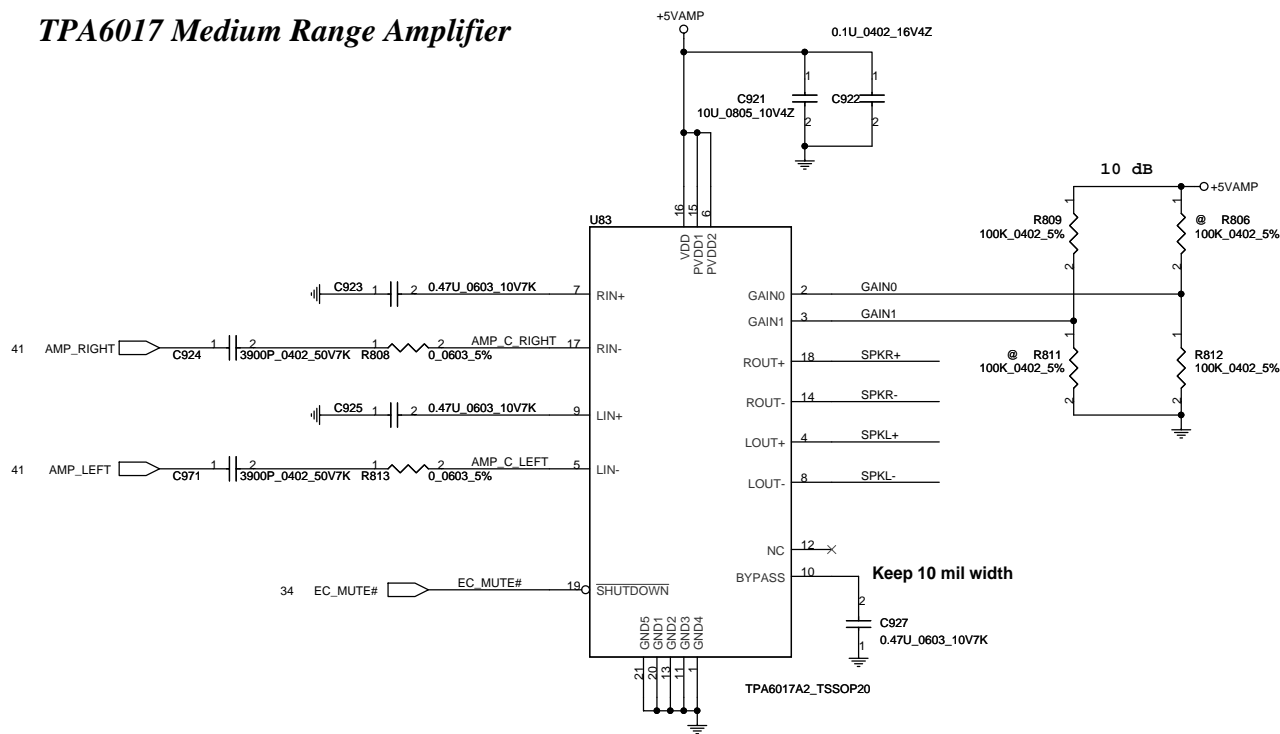
HD Audio Codec



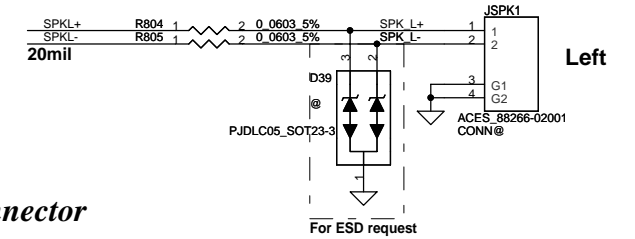
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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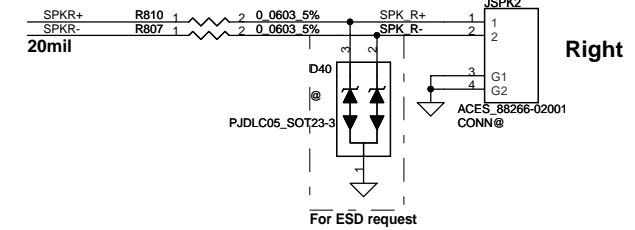
TPA6017 Medium Range Amplifier



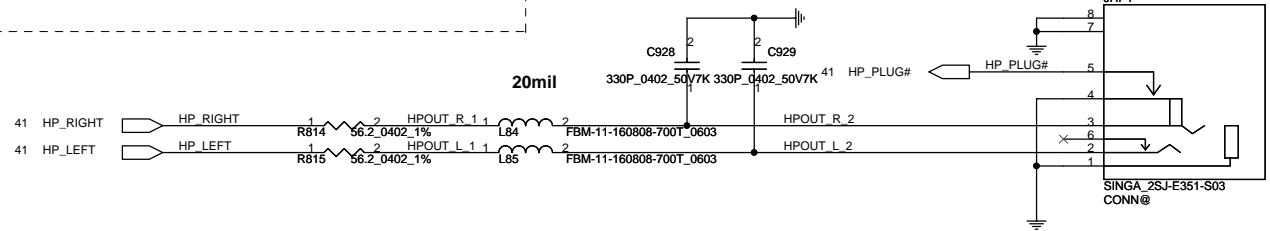
Left Connector



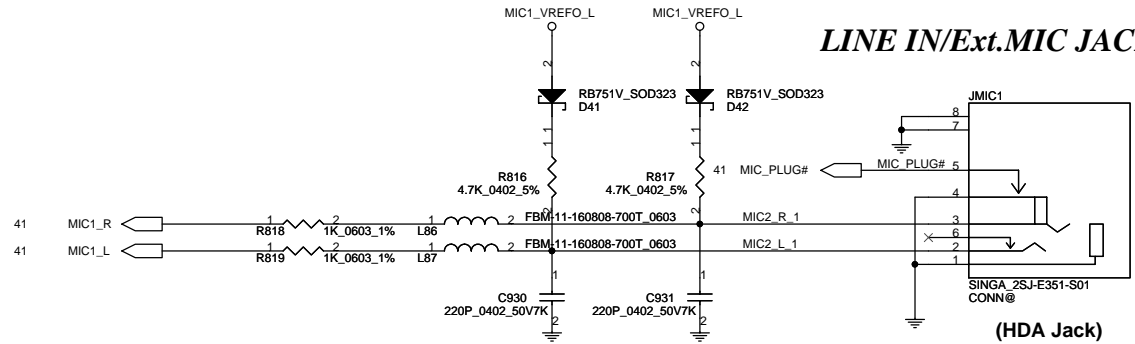
Right Connector



LINE Out/Headphone Out



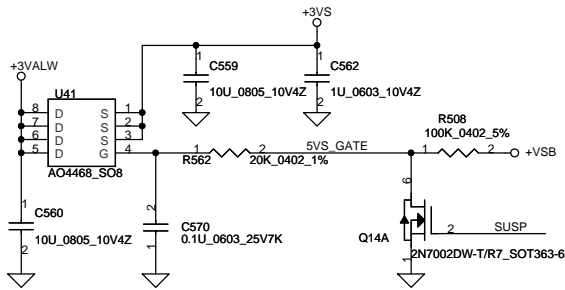
LINE IN/Ext.MIC JACK



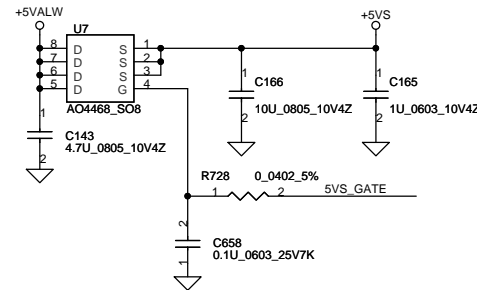
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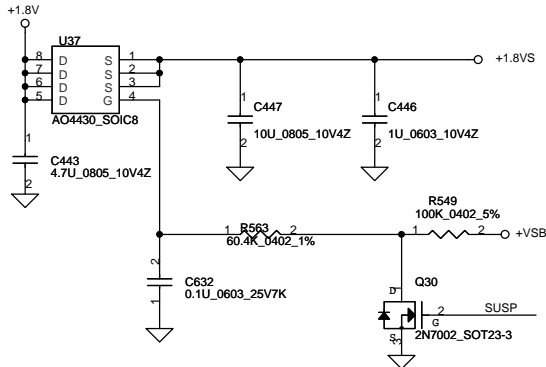
+3VALW TO +3VS



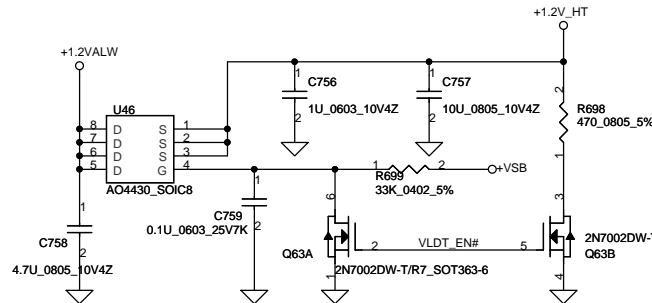
+5VALW TO +5VS



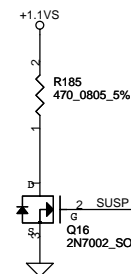
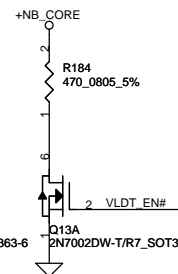
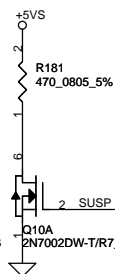
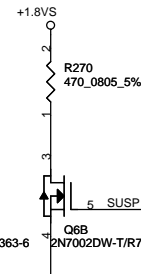
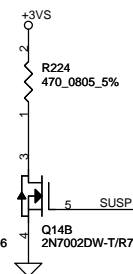
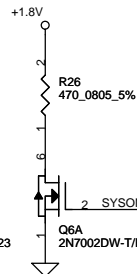
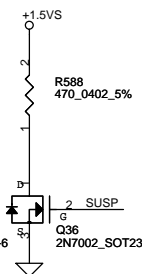
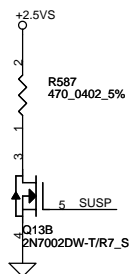
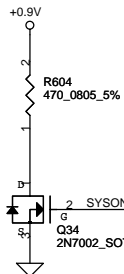
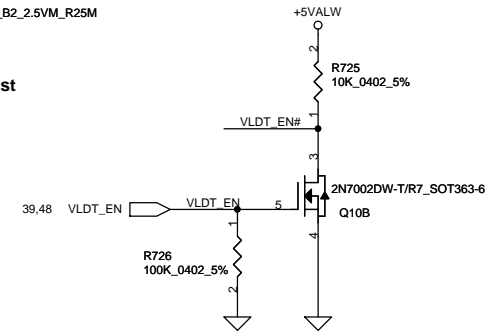
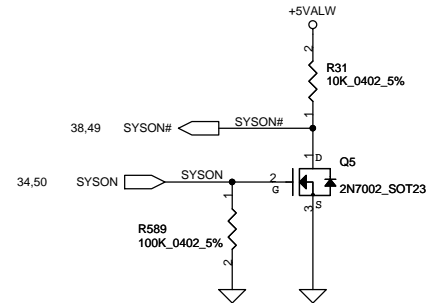
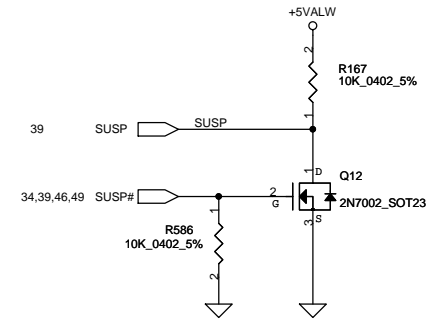
+1.8V TO +1.8VS



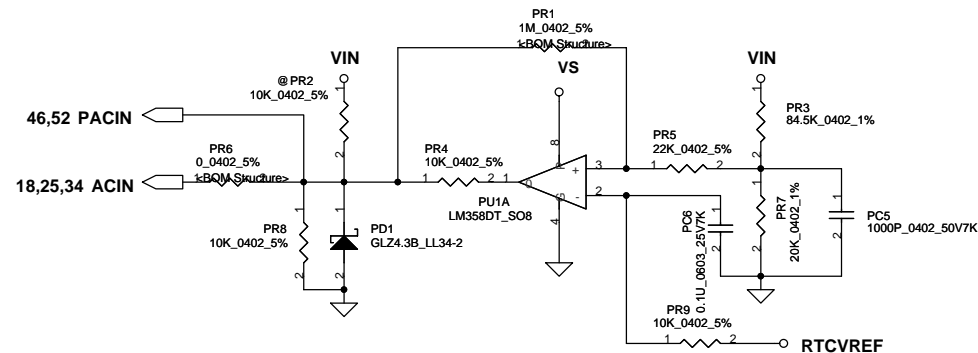
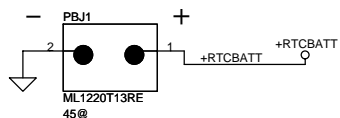
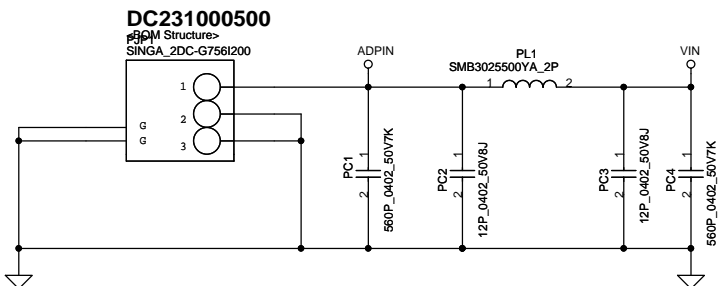
+1.2VALW TO +1.2V_HT



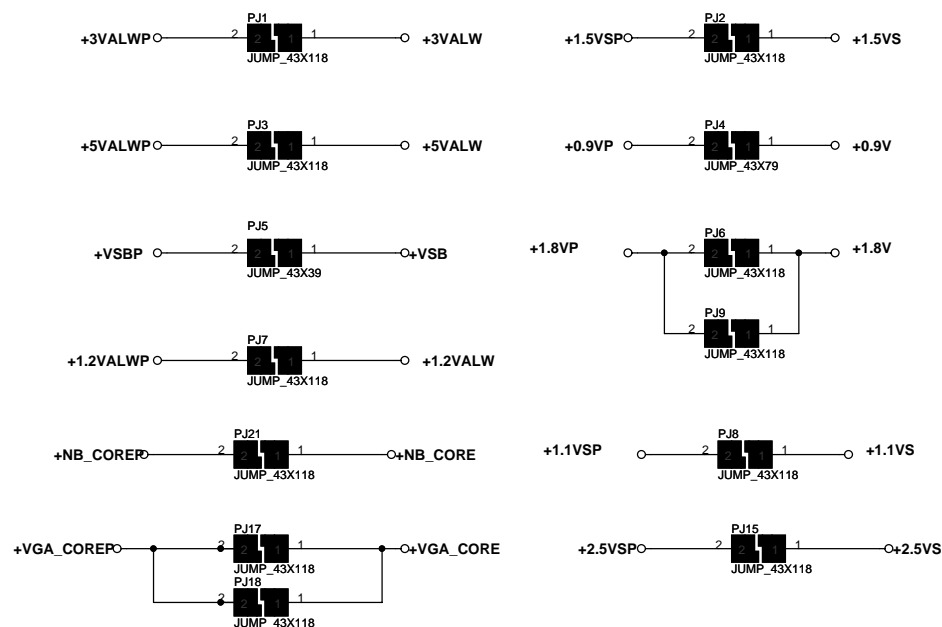
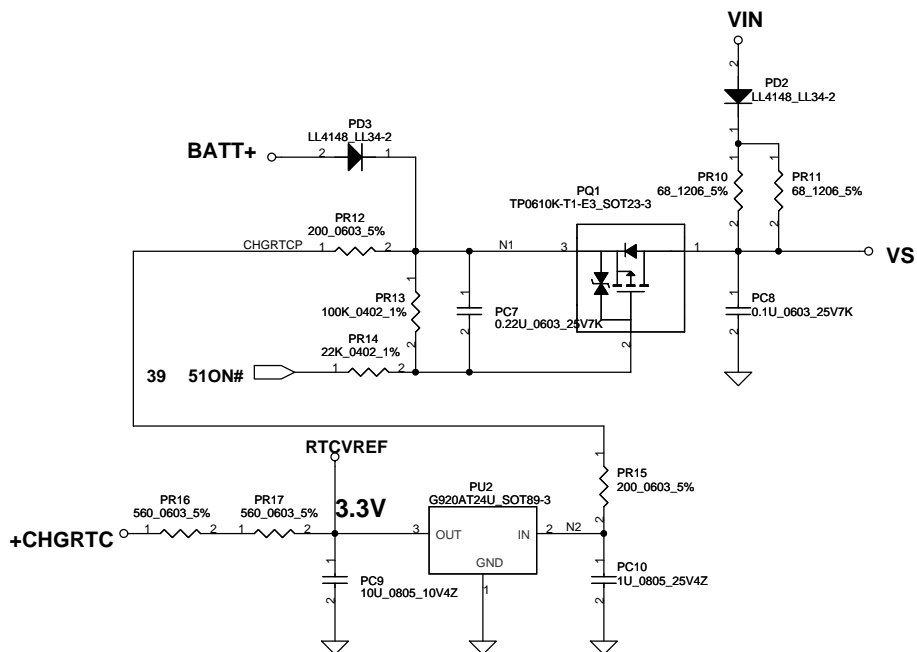
For PWR request



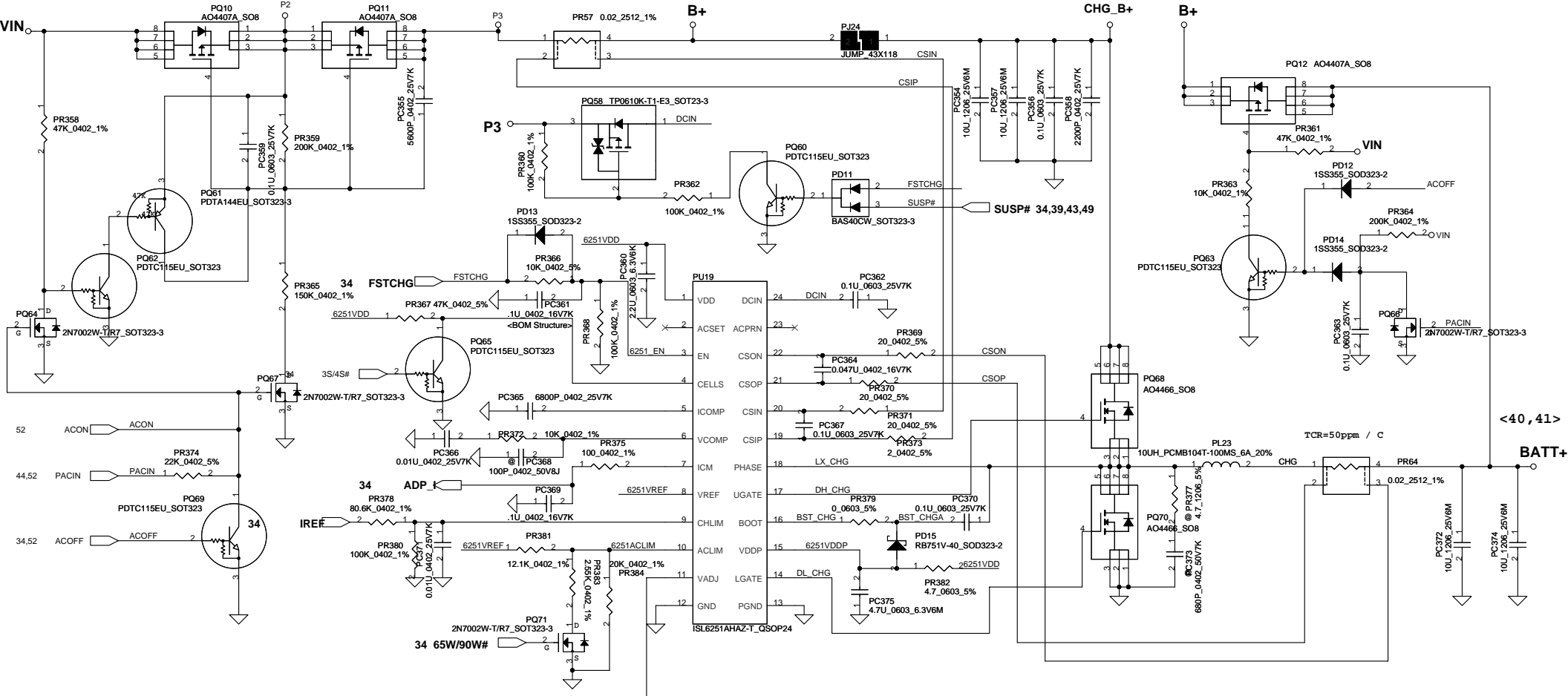
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Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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CP mode

$I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6~4.48A

$I_{ref} = 0.7224 * I_{charge}$
 $\Rightarrow K_i = 0.7224$
 $IREF = 0.43V \sim 3.24V$

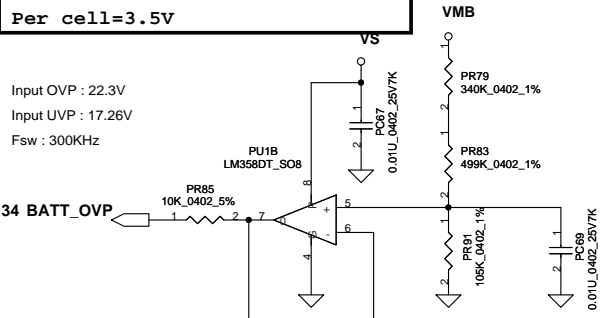
K_i
 $V_{chlim} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow K_i = 0.7224$

K_v
 $R_{internal} = 514K$ $R_{ec} = 3K$ $R_1 = PR379 = 15.4K$ $R_2 = PR381 = 31.6K$
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{cell} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * K_v = (4.2 - (4.2 + A * 0.175)) * K_v$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $K_v = 9.451$

LI-3S :13.5V---BATT-OVP=2.007V

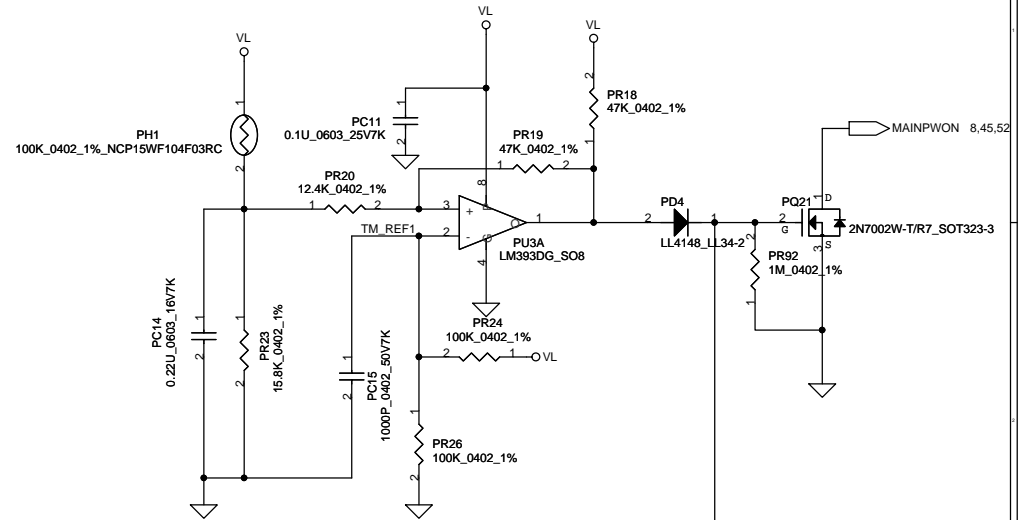
$BATT-OVP = 0.1487 * V_{MB}$
Per cell=3.5V

Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

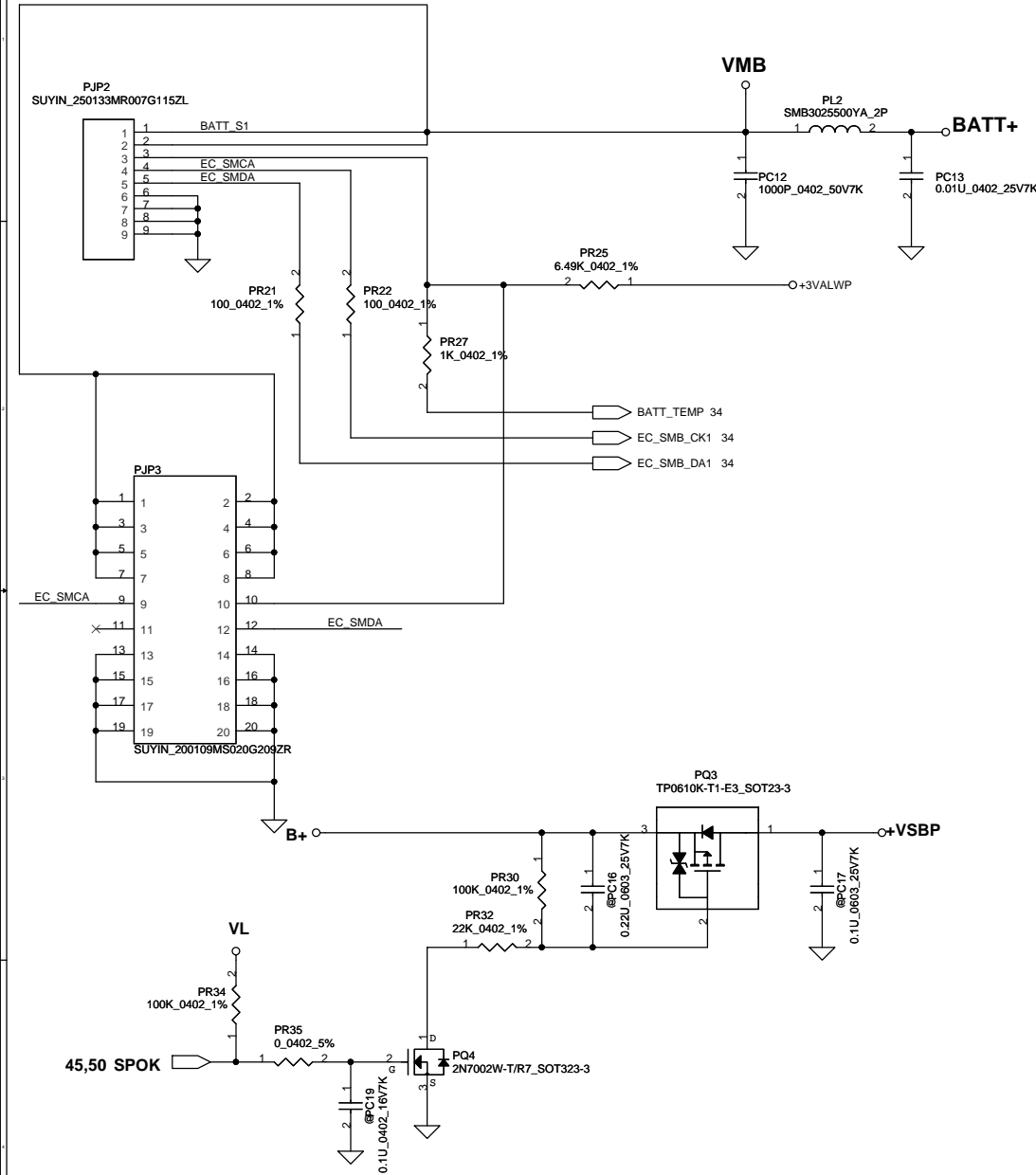
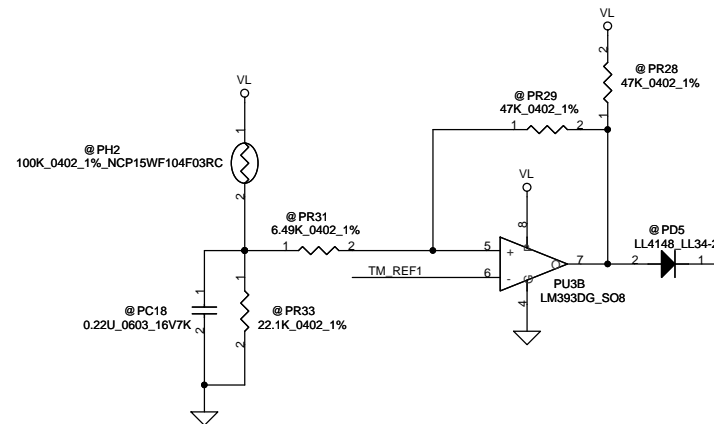


BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

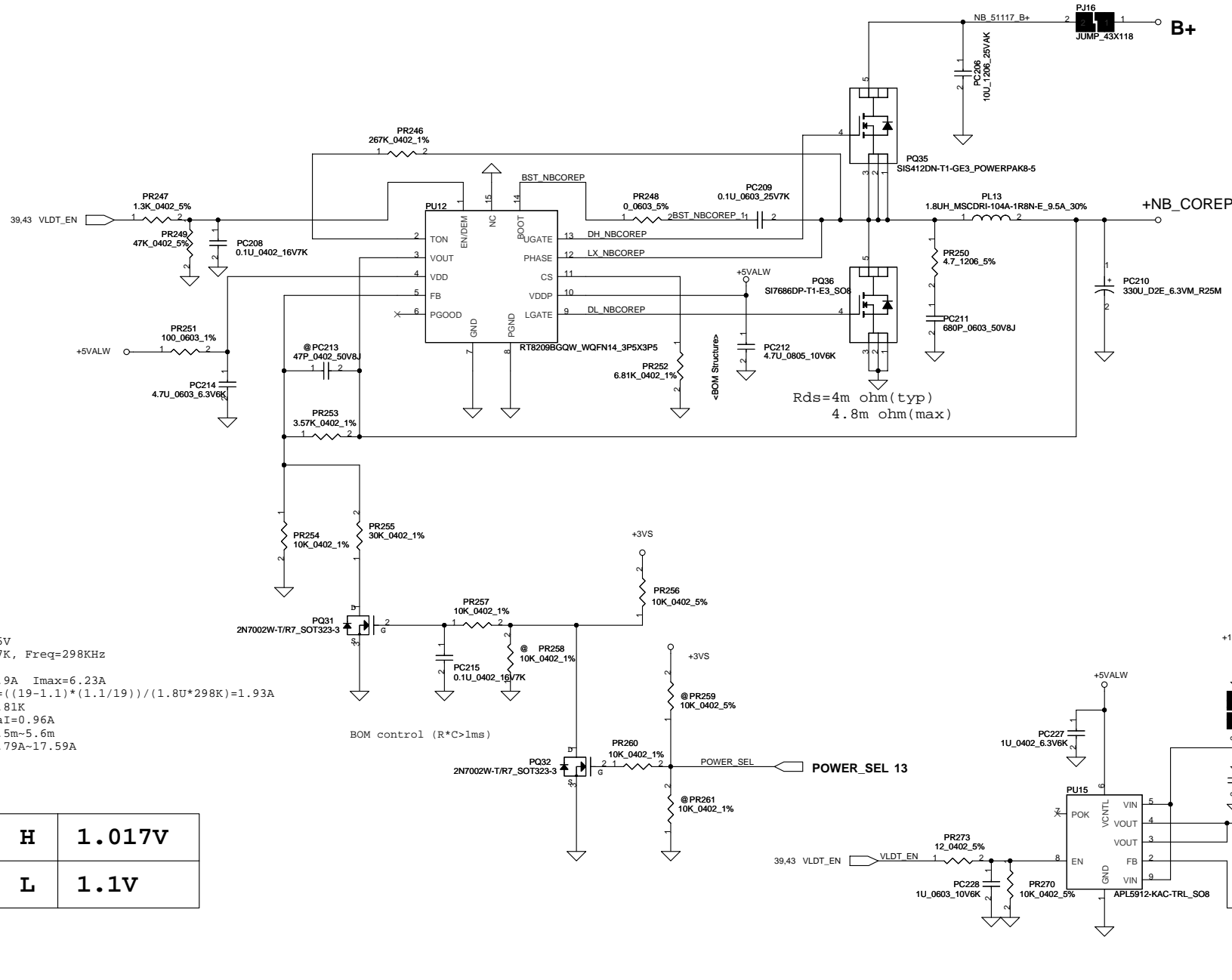
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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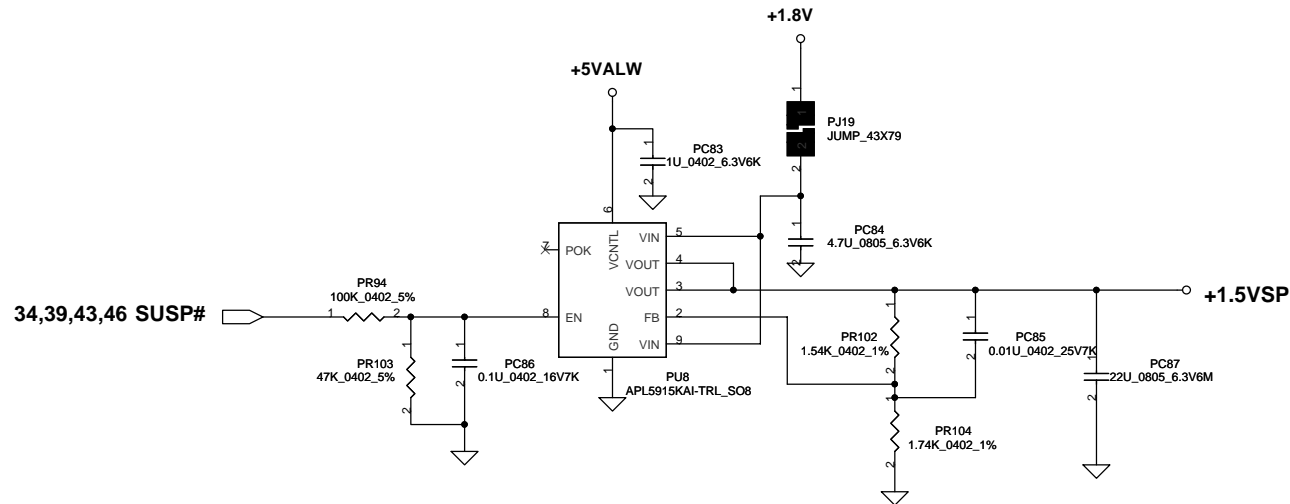
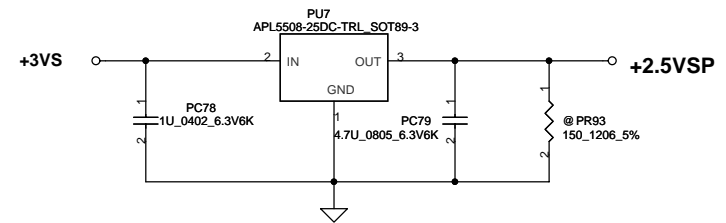
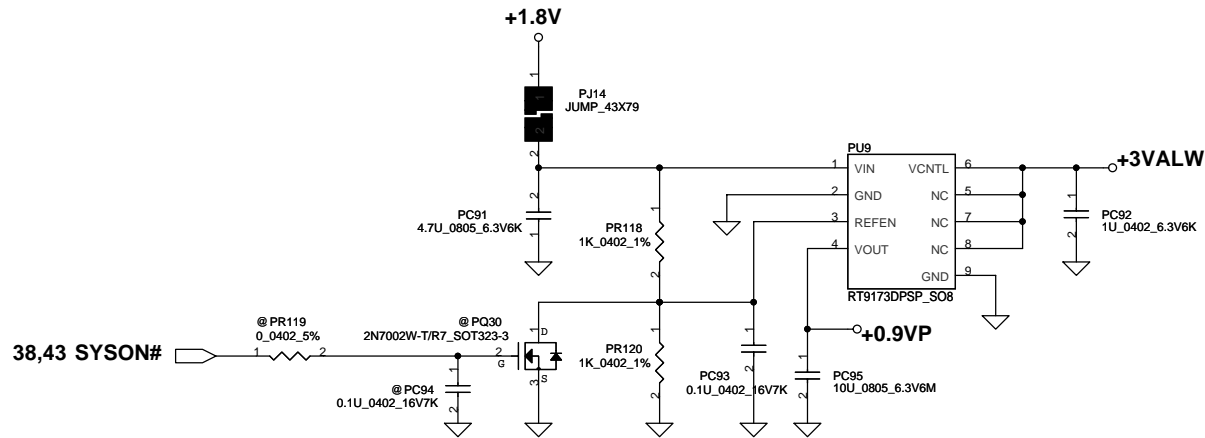


VFB=0.75V
Rton=267K, Freq=298KHz
Ipeak=8.9A Imax=6.23A
Delta I=((19-1.1)*(1.1/19))/(1.8U*298K)=1.93A
Rtrip=6.81K
1/2DeltaI=0.96A
Rdson=4.5m~5.6m
Iocp=10.79A~17.59A

BOM control (R*C>1ms)

H	1.017V
L	1.1V

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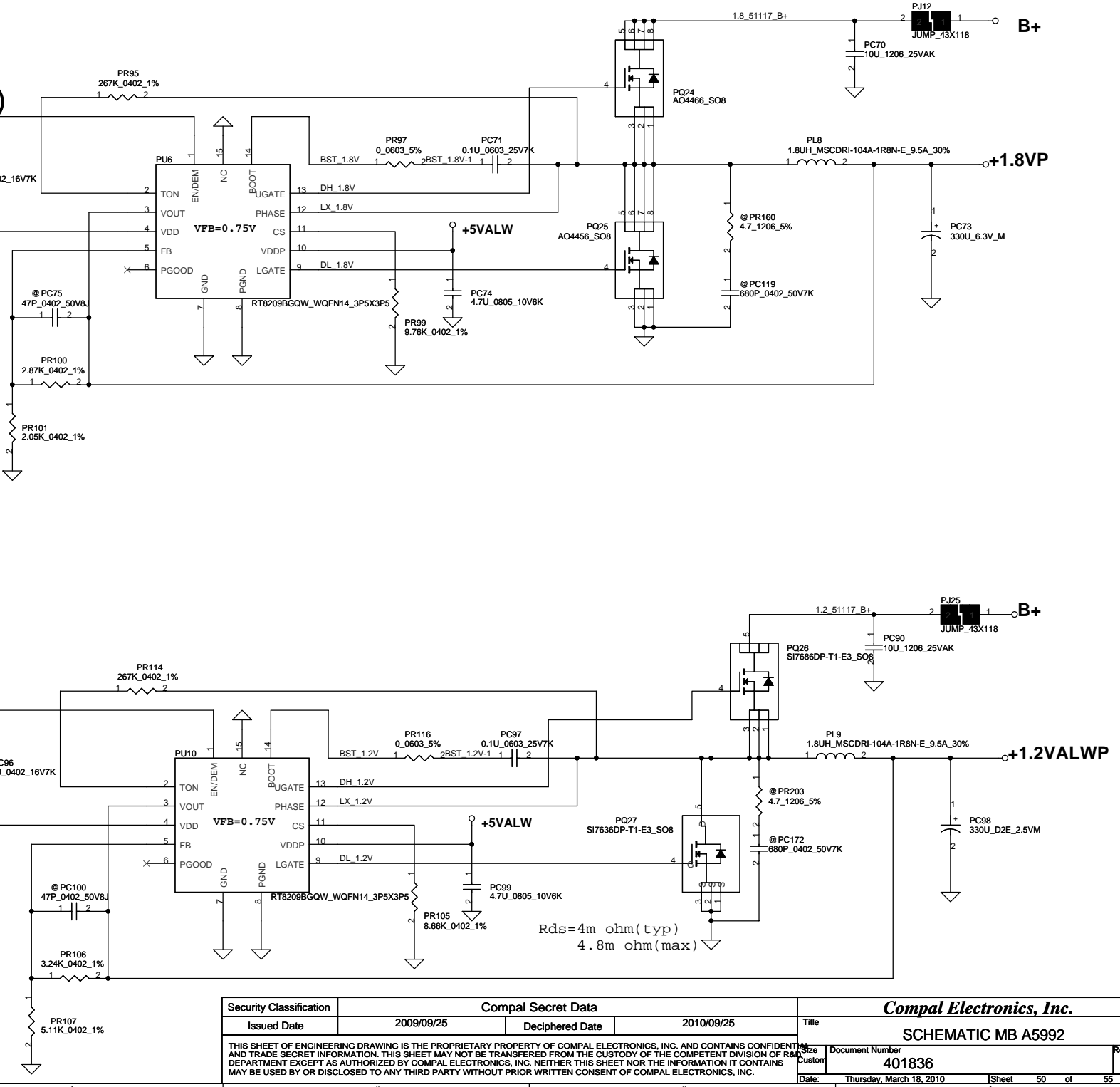
VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{aw} = 297KHz$

Cout ESR=15m ohm
 $I_{peak} = 11.96A$, $I_{max} = 8.372A$
 $\Delta I = ((19 - 1.8) * (1.8 / 19)) / (L * F_{sw})$
 $((19 - 1.8) * (1.8 / 19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1 / 2 \Delta I = 1.524A$
 $R_{trip} = 9.76K$
 $I_{ocp} = 15.20A - 24.71A$

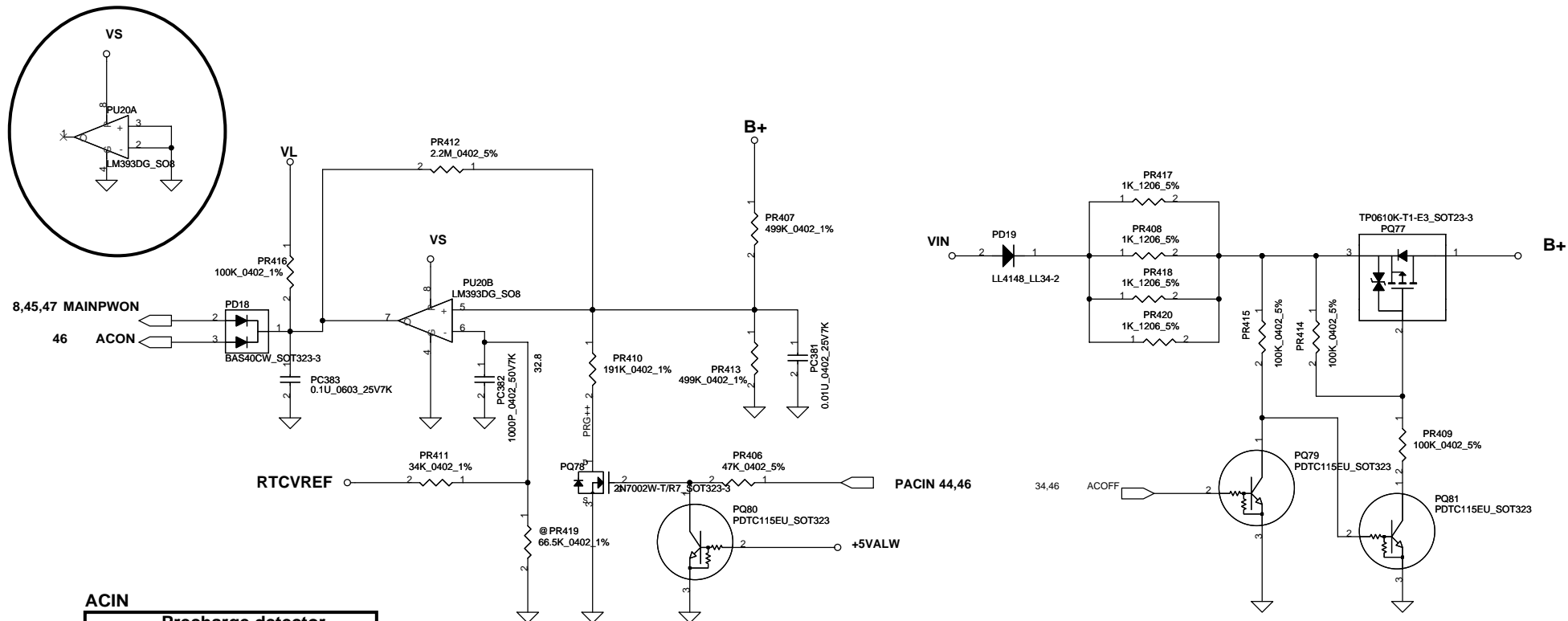
VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

1.2VP $I_{peak} = 7.4A$; $I_{max} = 5.180A$
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw})$
 $((19 - 1.2) * (1.2 / 19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1 / 2 \Delta I = 1.05A$
 $R_{ds(on)} = 15m / 18m \text{ ohm}$
 $set R_{trip} = 8.66K$
 $I_{ocp_min} = 4.77A$
 $I_{ocp_max} = 7.74A$

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ACIN

Precharge detector

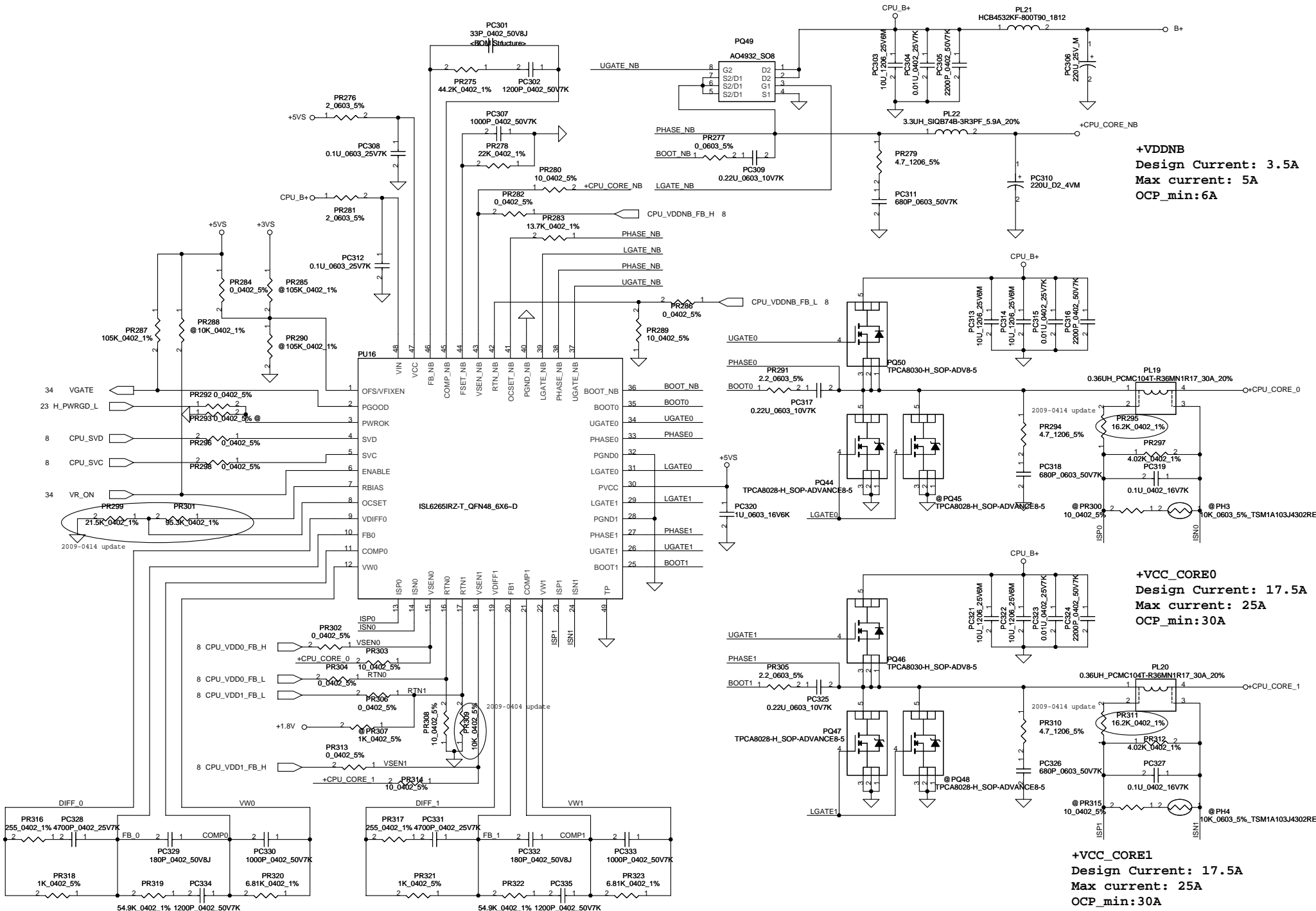
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector

	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be gitter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGAI9331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
7							
8	Change Power Source	For WLAN wakeup	1.0	37	Change R550 to +3VALW	09, 05/07	Pre-MP
9							
10							
11							
12							
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14							
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16							
17							
18							

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